Research Migration Project

https://esim.fossee.in/research-migration-project

Name of the participant : Vanjala Rajyalakshmi
Affiliation / Institution : Department of Electrical and communications Engineering,RGUKT Nuzvid,Andhra pradesh,India.

Title of the circuit : Design, Verification, and Comparative Power Evaluation of an RS(15, 11) Reed-Solomon Encoder using Operand Isolation.

Theory/Description : Reed-Solomon RS(15, 11) is a non-binary cyclic forward error-correcting (FEC) block code operating over Galois Field arithmetic GF(2^m).The circuit processes an 11-symbol input message sequence k = 11 and computes 4 parity check symbols 2t = n - k = 4 to construct a standard 15-symbol systematic codeword n = 15 via a Linear Feedback Shift Register (LFSR) architecture.

The design incorporates two distinct structural implementations co-simulated under identical clock, reset, and data stimuli:

- Baseline Architecture (rs_encoder_baseline): Standard LFSR datapath where internal Galois Field multiplier trees and XOR feedback networks switch continuously across all 15 clock cycles.
- Isolated Architecture (rs_encoder_isolated): Incorporates operand isolation (input gating) to hold multiplier inputs static (fixed to zero) during the initial 11-cycle message transmission phase, activating the feedback multiplier logic exclusively during the final 4 parity computation cycles.

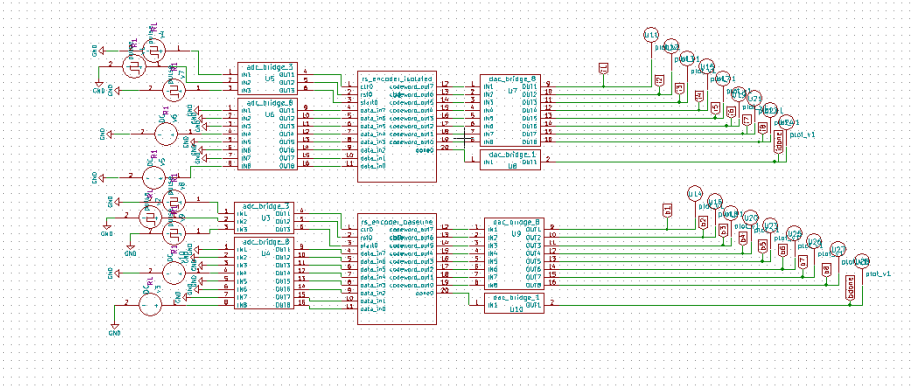
Reason to reproduce with eSim :

- Open-Source Mixed-Signal Verification: eSim integrates KiCad schematic capture, NgVeri (Icarus Verilog-to-XSPICE bridge), and the Ngspice simulation engine into a unified open-source workflow, eliminating the dependency on proprietary commercial EDA suites.
- Side-by-Side Co-Simulation: Enables simultaneous instantiations of baseline and optimized digital architectures within a single testbench, providing direct waveform comparison and signal integrity validation.
- Educational & Research Utility: Demonstrates practical low-power VLSI design methodologies—specifically operand isolation and dynamic switching activity reduction—in communication coding systems.

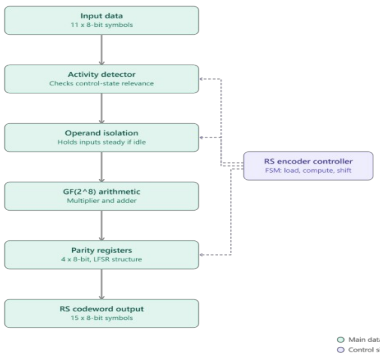
Expected Outcome/outputs :

- 100% Functional Equivalence: Both encoders produce identical 15-symbol codeword sequences across their respective 8-bit output buses (b1–b8 and i1–i8), confirming zero algorithmic degradation or bit errors.
- Zero Latency Penalty: Both architectures assert their completion flags (bdone and idone) synchronously after exactly 15 clock cycles 150 ns active duration at 100 MHz
- Output Signal Integrity: Identical output load power 6.84mW and packet transmission energy 0.957 nJ across equivalent load models) verify clean digital logic transitions 0V / 5V without timing jitter or voltage droop.
- Internal Switching Reduction: Multiplier active duty cycle is reduced from 100% 15/15 cycles down to 26.67% (4/15 cycles)establishing a theoretical 73.33% reduction in Galois Field multiplier dynamic switching activity.

Circuit Diagram(s) :



Block Diagram (s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :

Baseline RS(15,11) encoder:

- Input: 11 sequential 8-bit data symbols applied one per clock cycle (e.g., `01 02 03 04 05 06 07 08 09 0A 0B` in hex), synchronous to a system clock (10 ns period used in simulation, i.e. 100 MHz).
- Expected output: A 15-symbol codeword streamed on `codeword_out`, one 8-bit symbol per clock cycle — the first 11 symbols pass through unchanged (systematic encoding), followed by 4 computed parity symbols. For the test vector above, the expected parity symbols are `DE 85 69 32` (independently verified via a Python GF(2^8) reference model, not just the RTL itself).

Proposed (optimized) encoder vs. baseline:

- Functional equivalence: `codeword_out` from the proposed design must be bit-for-bit identical to the baseline's output for every test vector — this is the primary correctness result to demonstrate, shown as two overlapping/matching waveform traces.
- Switching activity reduction: measured via toggle count on internal multiplier signals (from VCD dump) during cycles where the activity detector holds operands isolated — expected to show a measurable reduction in toggle count on the isolated GF multiplier's internal nodes compared to the baseline, reported as a percentage.

Research Paper/Journal/etc. :

Title : Low-Power Design of Reed-Solomon Encoders .
Author : Wei Zhang, Jing Wang, Xinmiao Zhang
Link : https://ieeexplore.ieee.org/abstract/document/6572157

Source/Reference(s) : 1) I. S. Reed and G. Solomon, "Polynomial Codes Over Certain Finite Fields," *Journal of the Society for Industrial and Applied Mathematics*, vol. 8, no. 2, pp. 300–304, 1960. (foundational RS code theory)

2) Wei Zhang, Jing Wang, Xinmiao Zhang, "Low-Power Design of Reed-Solomon Encoders," IEEE. (primary related-work reference, see prior message