Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : Dhruv Mittal

Affiliation / Institution : Department of Electrical Engineering, ZHCET, AMU, Aligarh, Uttar Pradesh, India

Title of the circuit : Memristor Emulator Circuit using Off-the-shelf Solid State Components (Op-Amp, Analog Multiplier and Current Mirrors) — Decremental Configuration

Theory/Description : A Memristor is the 4th fundamental circuit element which remembers how much current has passed through it. It has programmable resistance , in memristor the current and voltage relationship is defined as $v(t) = R(t) * i(t) = d\phi/dq * i(t)$ where ϕ(t) and q(t) denote the flux and charge, respectively, at time t.Since the ideal memristors are difficult to manufacture and are not commercially available,this circuit reproduces memristor behaviour using the standard off-the-shelf components.

Reason to reproduce with eSim : This circuit is well suited to be reproduced with eSim because it can be built entirely using the standard, off-the-shelf solid state components - all of which are natively supported in eSim's Ngspice based simulation environment.Reproducing this circuit in esim demonstrates the tool's capability to handle non-trivial mixed analog building blocks,including current-mirror networks and a custom four quadrant analog multiplier(implemented as a behavioural subcircuit)

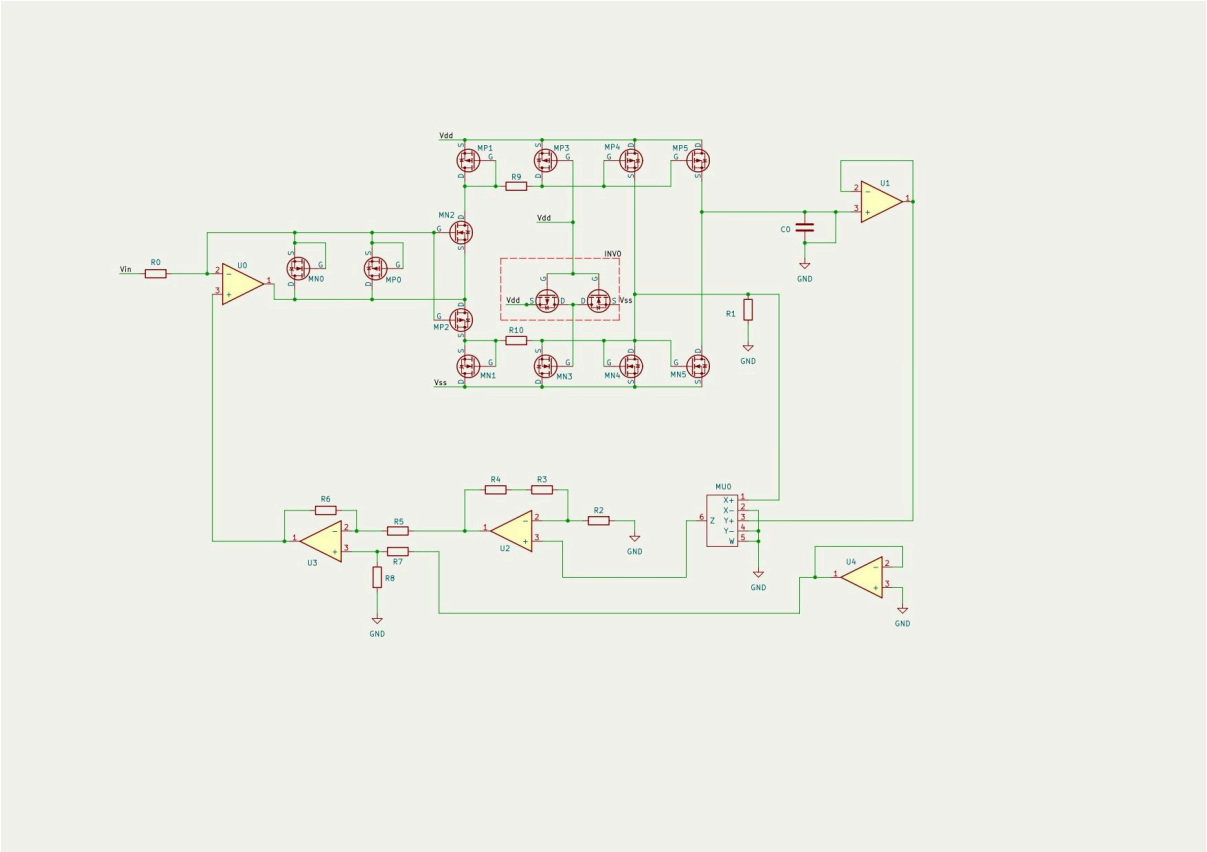
Expected Outcome/outputs : On simulating the circuit in eSim, the following behaviors are expected, consistent with the results reported in the original paper:

1. A pinched hysteresis loop in the voltage-current (V-I) plane when a sinusoidal input (100 Hz, 2 Vp-p) is applied to Vin — the defining signature of memristive behavior, arising from the charge-dependent resistance implemented via the capacitor-multiplier feedback path.
2. Frequency-dependent narrowing of the hysteresis loop as the input frequency is increased (tested at 100 Hz, 200 Hz, 400 Hz, and 800 Hz), confirming the frequency-dependent nature of the emulated memristance.
3. Non-volatility of the memristance state — when a rectangular pulse train (0.1 V, 2.5 ms duration, 10 s period) is applied, the memristance is expected to change in discrete steps only during the pulses and remain constant during idle periods,

verifying that the charge stored on capacitor C0 is retained (buffered by op-amp U1) rather than discharging.

4. Overall validation that the circuit's input resistance decreases progressively with accumulated charge, consistent with the decremental memristor emulator configuration.

Circuit Diagram(s) :

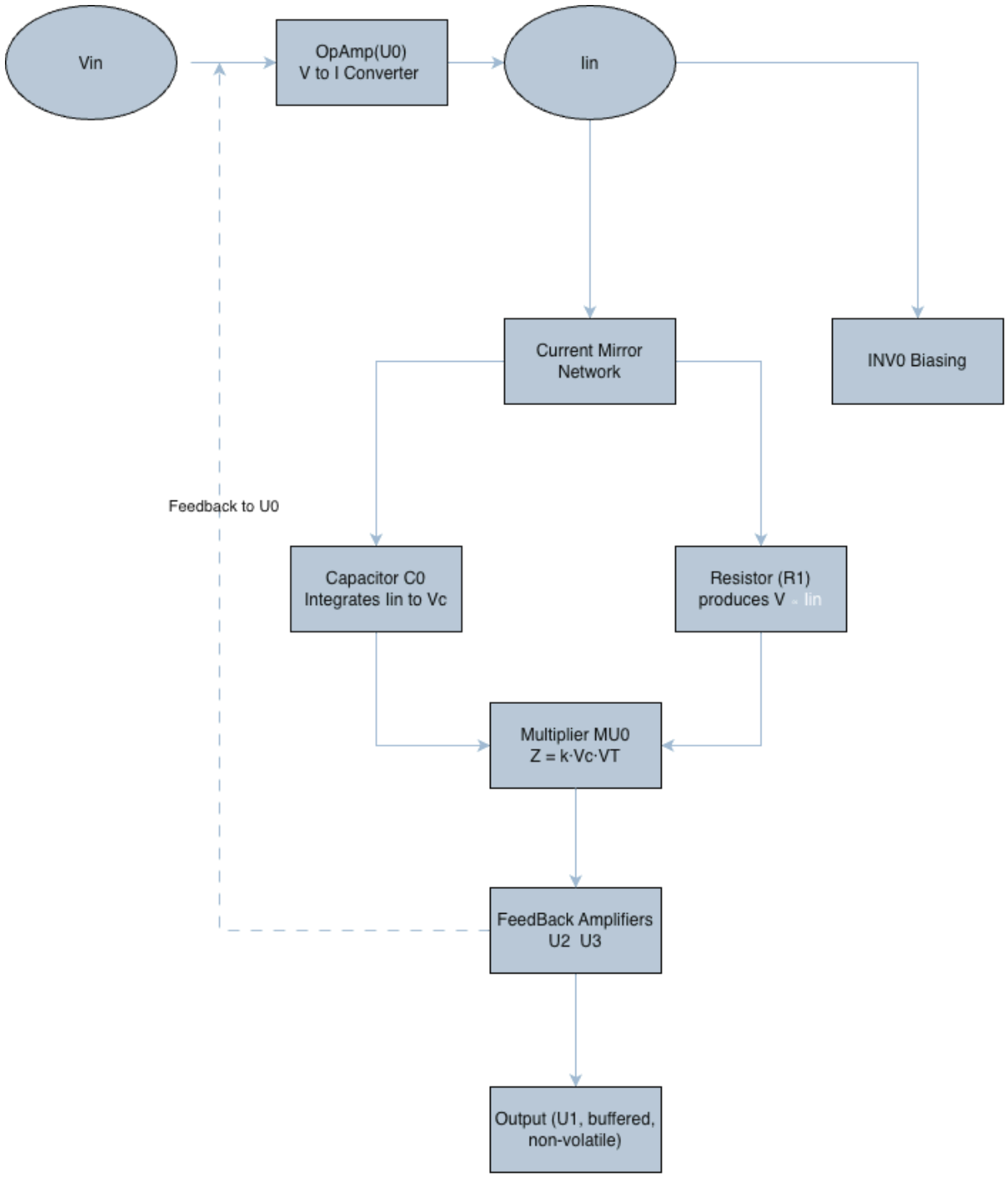


The circuit was implemented in eSim following the full schematic of Fig. 5 of the reference paper (decremental memristor emulator configuration), consisting of:

- A voltage-to-current converter stage (R0, U0, and transistors MN0/MP0) that converts the input voltage Vin into a proportional current using the virtual-ground property of the op-amp.
- A current-mirror network built from matched NMOS transistors (MN1–MN5) and PMOS transistors (MP1–MP5), biased through resistors R9 and R10, which replicates and splits the bidirectional input current into separate positive and negative signal paths.
- A CMOS inverter (INV0), biased from the Vss rail, which sets the polarity of the current-mirror biasing to configure the circuit in the decremental mode.
- An integrator stage (capacitor C0) that stores the time-integral of the input current as a voltage, buffered through op-amp U1 to preserve the stored charge and provide non-volatility.

- A sensing resistor (R1/RT) that produces a voltage proportional to the instantaneous current.
- A custom four-quadrant analog multiplier subcircuit (MU0), implemented in eSim using a behavioral (B-source) SPICE model with pins X+, X−, Y+, Y−, W, and Z, which computes the product of the capacitor voltage and the RT voltage to realize the charge-dependent resistance term of the memristor equation.
- A feedback conditioning network (op-amps U2, U3, U4 with resistors R2–R8) that scales and routes the multiplier output back to the input stage (U0), closing the loop that makes the effective input resistance a function of the accumulated charge.
- Supply rails Vdd = +5 V and Vss = −5 V.

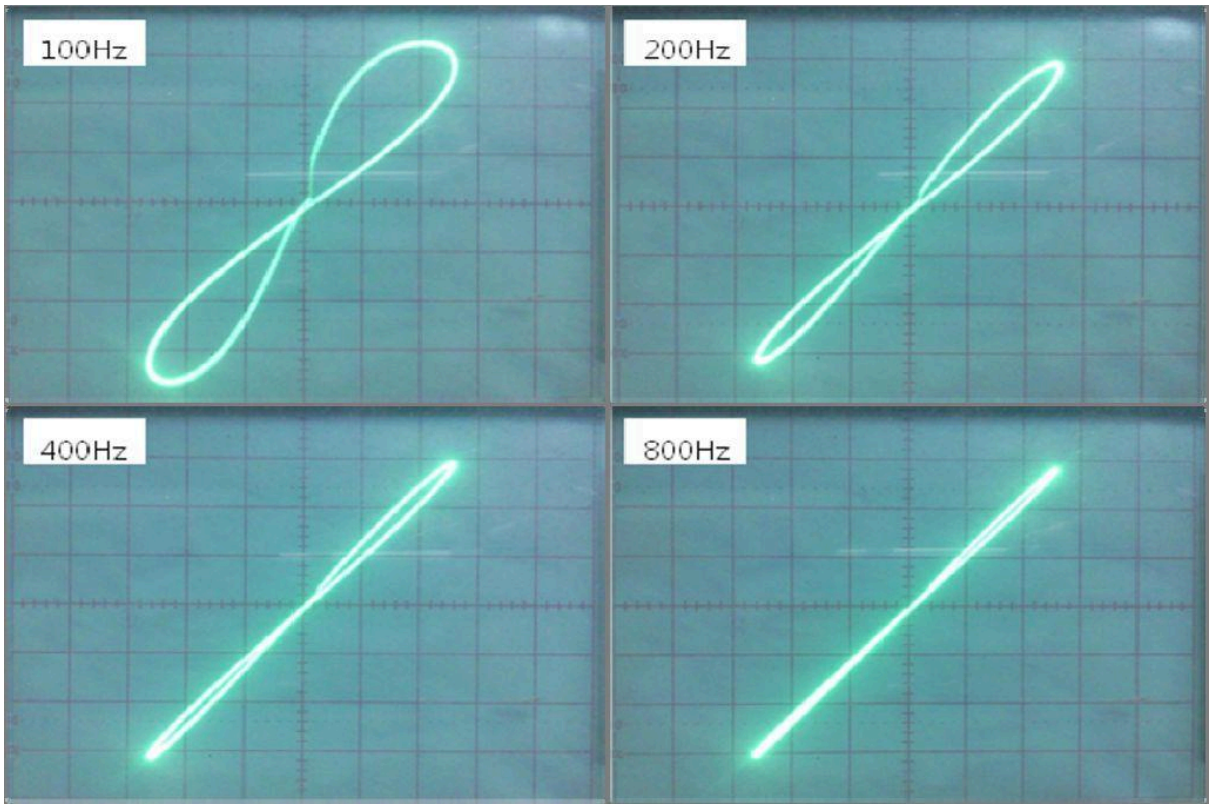
Block Diagram (s) :

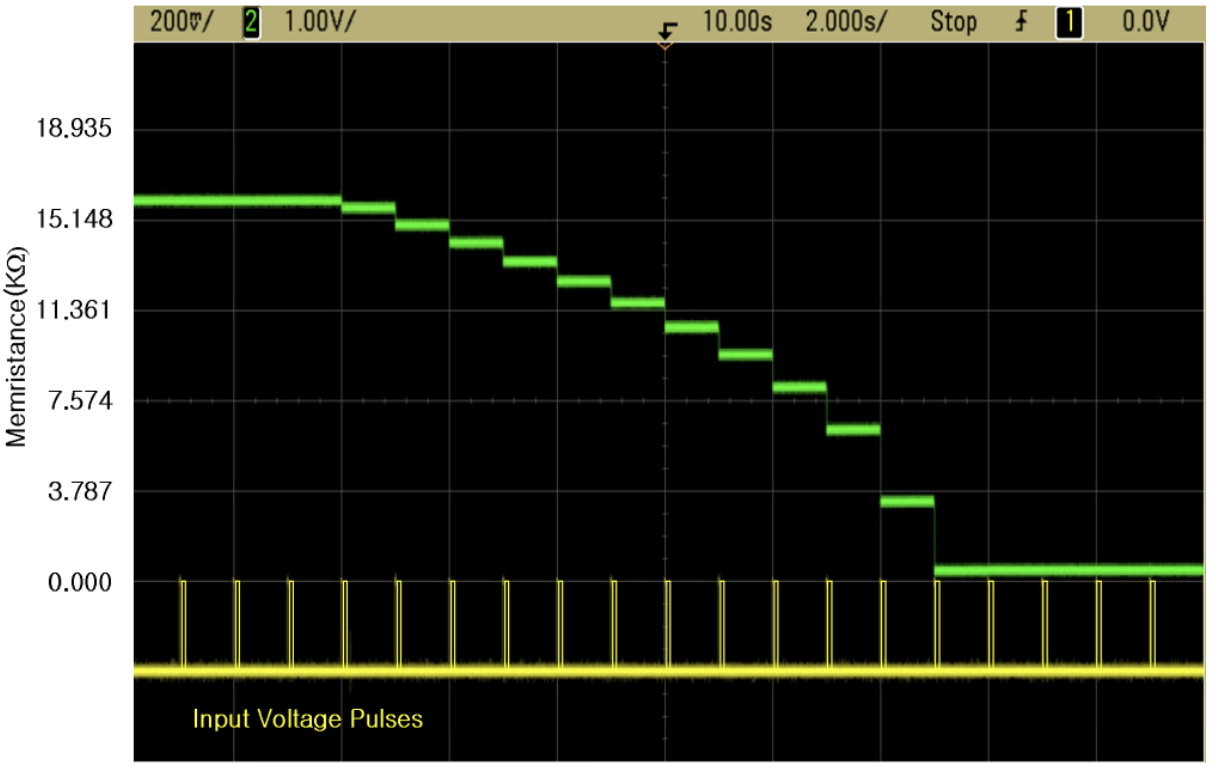


Expected Results (Input, Output waveforms and/or Multimeter readings) :

- **Input:** Sinusoidal voltage source, 2 Vp-p amplitude, frequency swept across 100 Hz, 200 Hz, 400 Hz, and 800 Hz.
- **Output:** V-I characteristic plot (obtained from the research paper) showing a pinched hysteresis loop passing through the origin at every tested frequency, with loop width decreasing as frequency increases.
- **Memristance readout**: Voltage at the output of U1 tracked over time, expected to vary within a bounded range (approx. 0–19 kΩ equivalent, Fig. 8 of the reference paper) as a function of applied charge.
- **Non-volatility test:** Rectangular pulse input (0.1 V, 2.5 ms duration, repeated every 10 s); output expected to show a step-wise decreasing memristance with flat, constant segments between pulses.

Supply: Vdd = +5 V, Vss = −5 V (DC sources).





Research Paper/Journal/etc. :

Title : Memristor Emulator with Off-the-shelf Solid State Components for Memristor Application Circuits
Author : Changju Yang, Seongik Cho, Maheshwar Pd. Sah, Hyongsuk Kim, Ki-Sang Jung
Link : https://ieeexplore.ieee.org/document/6331432

Source/Reference(s) :

- D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.
- L. O. Chua, "Memristor—the missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.
- eSim User Manual, FOSSEE, IIT Bombay — used for schematic creation, Subcircuit Builder, and Ngspice conversion workflow.
- Ngspice Manual — reference for behavioral (B-source) modeling used to implement the four-quadrant analog multiplier subcircuit

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Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.