Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit :

Design and Simulation of a conventional 1T1C DRAM Sensing Circuit and a Redundant Voltage Discharged Single Bitline Load Sense Amplifier (RVD-SBLSA)

Theory/Description :

A 1T1C DRAM cell stores one bit of data in the form of charge on a capacitor (Cs). An NMOS transistor is used to connect the capacitor to the bitline, and this transistor is controlled by the wordline (WL). Since the stored charge is very small, the data cannot be read directly. A sense amplifier is therefore used to detect and amplify the small voltage difference produced on the bitline.

Before a read operation, the bitline pair (BL and BLB) is precharged to around VDD/2 using NMOS transistors controlled by the PRE signal. When the wordline is activated, the charge stored in the capacitor shares with the bitline capacitance. This creates a small voltage difference between BL and BLB. The cross-coupled CMOS inverters in the sense amplifier then amplify this small difference and drive the bitlines to full logic levels. At the same time, the original data in the DRAM cell gets restored, so the sensing operation also performs the refresh of the cell.

The RVD-SBLSA proposed in the paper is a modified version of the conventional sense amplifier. It uses additional switches (N4/P4 and N5/P5) to separate the reference bitline from the sense amplifier during sensing. It also uses two diode-connected NMOS transistors (N6 and N7) to control the bitline voltage during the discharge operation. The main idea is to reduce the unnecessary energy used for bringing the reference bitline from VDD back to VDD/2 after sensing.

Reason to reproduce with eSim :

Sense amplifiers are an important part of DRAM because they are involved in every read operation and can contribute significantly to the overall power consumption. Reproducing

both the conventional sense amplifier and the RVD-SBLSA in eSim would give a good way to understand how the circuit works and to compare their power and voltage behaviour.

The circuits mainly use standard NMOS and PMOS transistors, which makes them suitable for implementation using the devices available in eSim and ngspice. The original work uses a 65 nm technology, but reproducing the circuit in eSim does not require using the same proprietary technology. Instead, the main circuit operation and the claimed improvement can be studied using an open-source simulation environment. This would also make the design easier for other students to understand, simulate and modify.

Expected Outcome/outputs :

Both the conventional sense amplifier and the RVD-SBLSA will be tested for different DRAM operations, including read '0', read '1', read '0'-write '1', and read '1'-write '0'. For each case, the simulation will follow the same basic sequence used in the paper, starting with precharge and sensing, followed by the post-sense operation and I/O transition. For the RVD-SBLSA, the additional discharge stage will also be included before the next precharge cycle.

The supply current obtained from the transient simulation will be used to estimate the energy consumed during each operation. The main purpose is to compare the two sense amplifiers rather than to obtain exactly the same energy values as the original paper. Based on the results reported in the paper, the RVD-SBLSA is expected to use less energy than the conventional sense amplifier, especially during read '1', read '0'-write '1', and read '1'-write '0' operations.

The original circuit was designed using a 65 nm technology, while eSim/ngspice will use the available generic transistor models. Because of this difference, the exact voltage and energy values may not be the same as those reported in the paper. However, the main waveforms, circuit operation, and overall power-saving trend can still be compared. The aim is to check whether the RVD-SBLSA shows the expected reduction in energy compared with the conventional design.

Circuit Diagram(s) :

The two circuits that will be reproduced are shown below. The first one is the conventional 1T1C DRAM sense amplifier circuit, and the second one is the RVD-SBLSA circuit given in the reference paper. These circuits will be used as the main reference while creating the corresponding schematics in eSim. The transistor sizes and other circuit parameters will be decided and adjusted during the implementation and simulation stage.

Figure 1 (conventional sensing circuit, reproduced from Dai et al., 2023):

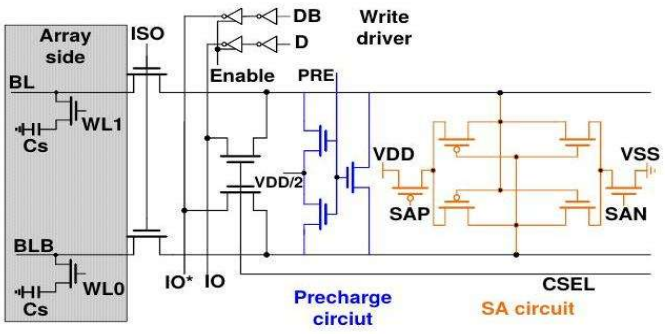
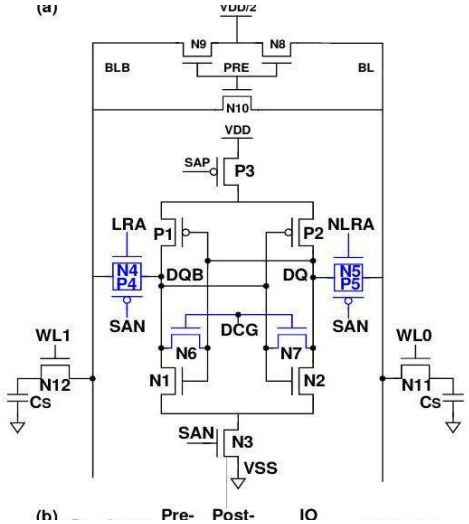
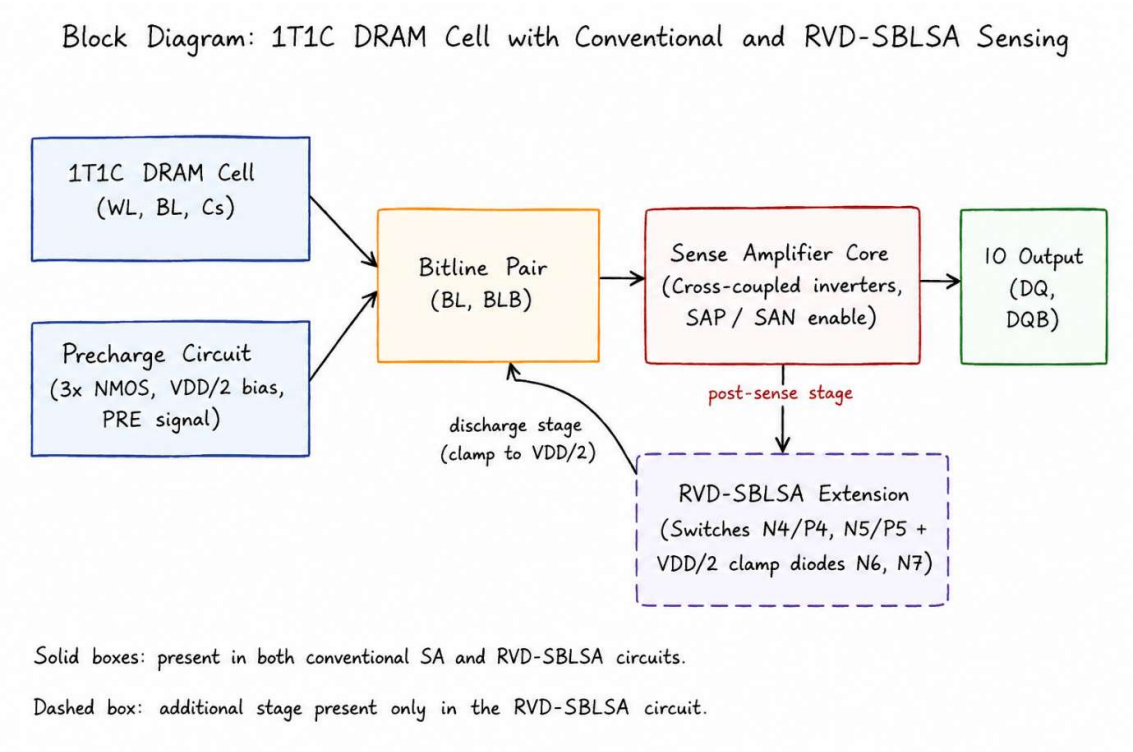


Figure 2 (RVD-SBLSA circuit, reproduced from Dai et al., 2023):



Block Diagram (s) :



Expected Results :

The main result will be the BL and BLB voltage waveforms for all four operations: read '0', read '1', read '0'-write '1', and read '1'-write '0'. The waveforms will be checked to see whether they follow the same basic behaviour as the reference paper. During precharge, both bitlines should come close to VDD/2. When WL is turned ON, a small voltage difference should appear because of charge sharing between the storage capacitor and the bitline. The sense amplifier should then increase this small difference and drive the bitlines towards 0 V or VDD.

For the RVD-SBLSA, the discharge part of the operation will also be observed. The reference bitline should move back towards VDD/2 during this stage before the next precharge cycle. The simulated waveforms will be checked at different stages to make sure that the circuit is working as expected. The energy used by both circuits will also be compared by using the transient supply current from the simulations.

Research Paper/Journal/etc. :

Title: Low-Power Single Bitline Load Sense Amplifier for DRAM
Authors: Chenghu Dai, Yixiao Lu, Wenjuan Lu, Zhiting Lin, Xiulong Wu, Chunyu Peng
Journal: Electronics, 2023, 12, 4024
Pages: 1–12

Source/Reference(s) :

DOI: https://doi.org/10.3390/electronics12194024

Other References

- **eSim/ngspice documentation: https://esim.fossee.in**
- **N. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* — used for understanding the conventional CMOS sense amplifier and for taking a baseline approach to transistor sizing.**
