FOSSEE Research migration project using eSim

Affiliation / Institution

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Title of the Circuit

Dual Flip-Flop Synchronizer for Clock Domain Crossing with Metastability Analysis

Theory / Description

- Clock Domain Crossing (CDC) occurs when a signal generated in one clock domain is transferred to another clock domain having a different clock or phase.
- Direct transfer of an asynchronous signal can cause **metastability** in the receiving flip-flop.
- A dual flip-flop synchronizer is used to reduce the probability of metastability propagating into the destination logic.
- The synchronizer consists of two D-type flip-flops connected in series and operated using the destination clock.
- The asynchronous input is applied to the first flip-flop. Its output is connected to the input of the second flip-flop.
- If the first flip-flop becomes metastable because of a setup or hold-time violation, the extra clock period allows the signal more time to settle.
- The output of the second flip-flop is used as the synchronized signal in the destination clock domain.
- The circuit can be simulated in eSim to observe the input signal, intermediate signal, synchronized output, and timing relationship between the clocks.

Reason to Reproduce with eSim

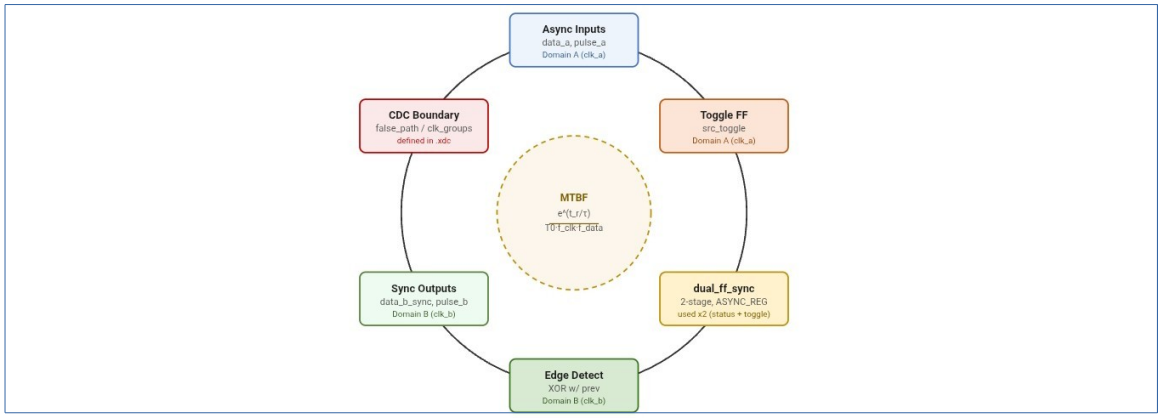
- eSim provides an open-source environment for designing and simulating the synchronizer using digital circuit components.
- The two flip-flop stages can be constructed and verified separately.
- Simulation makes it possible to observe the propagation of an asynchronous signal through both stages.
- Input, first flip-flop output, and final synchronized output can be observed using waveforms.
- Different clock frequencies and phase relationships can be studied.
- The simulation gives a simple understanding of metastability reduction and safe signal transfer between clock domains.

Expected Outcome / Outputs

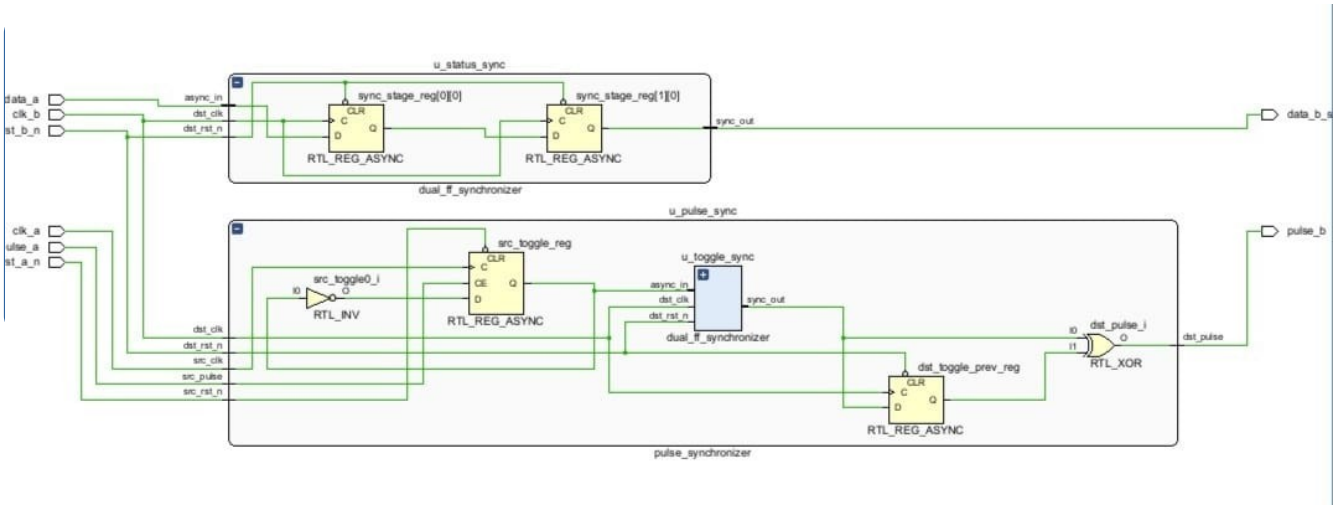
- Apply an asynchronous digital input signal to the synchronizer.
- The first flip-flop samples the asynchronous input using the destination clock.

• The second flip-flop samples the output of the first flip-flop on the next clock edge.
• The final output should be a stable synchronized version of the input.
• The synchronized output should show the expected clock-cycle delay.
• The circuit should demonstrate reduced propagation of metastability to the destination logic.

Dual Flip-Flop Synchronizer Block Diagram



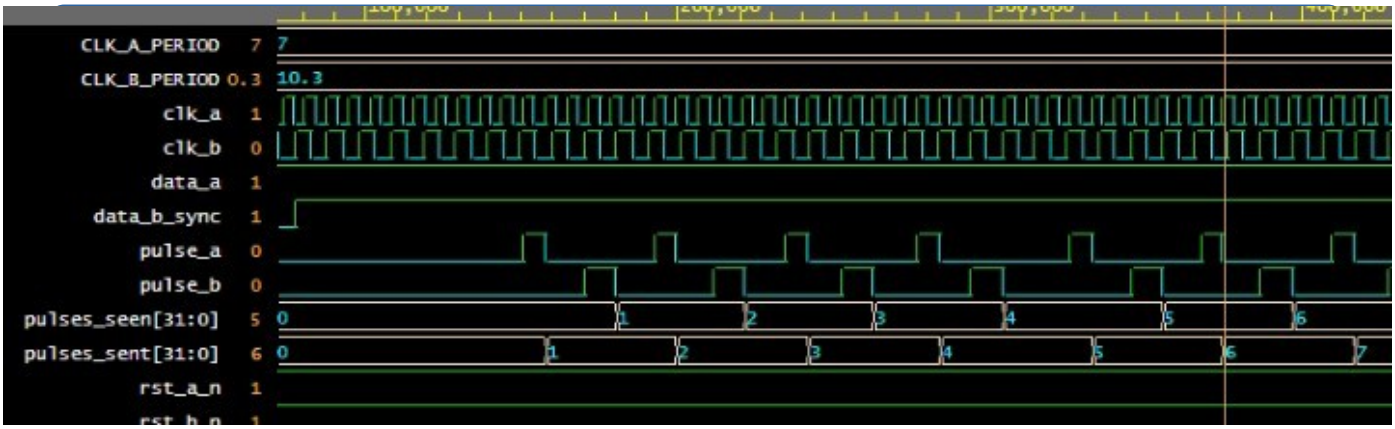
Circuit Diagrams



Expected Waveforms

• The waveform should show the asynchronous input signal and the destination clock.
• The output of the first flip-flop represents the intermediate synchronization stage.
• The output of the second flip-flop provides the stable synchronized signal.
• A delay of approximately two destination-clock sampling stages should be observed between the input transition and synchronized output.
• The waveform can be used to verify the correct operation of the synchronizer.

Expected Input and Output Waveforms



Expected Results

• An asynchronous digital signal is applied as the input.
• The first flip-flop samples the input using the destination clock.
• The second flip-flop produces the synchronized output.
• The synchronized output follows the input with the expected clock-cycle delay.
• The first-stage output may show an uncertain transition when the input changes close to the clock edge.
• The second-stage output should remain stable and suitable for use by the destination logic.
• The input and synchronized output waveforms are compared to verify correct operation.

Metastability Analysis

• Metastability may occur when the asynchronous input changes close to the active edge of the destination clock.
• The first flip-flop is the stage most likely to enter a metastable condition.
• The second flip-flop provides additional settling time before the signal reaches the destination logic.
• Therefore, the probability of metastability propagating to the destination logic is significantly reduced.
• The simulation can be used to observe the timing relationship between the asynchronous input, first-stage output, and synchronized output.

Research Paper / Journal Reference

• C. E. Cummings, “Clock Domain Crossing (CDC) Design & Verification Techniques Using SystemVerilog,” SNUG, 2008.
• T. J. Chaney and C. E. Molnar, “Anomalous Behavior ofSynchronizer and Arbiter Circuits,” IEEE Transactions on Computers, 1973.