Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit: Design and Simulation of a Glitch-Free Clock Multiplexer for Non-Continuously Running Clocks Using eSim

Theory/Description: A clock multiplexer is used to switch between two clock signals in a digital system. During switching, unwanted glitches or extra pulses can occur at the output, which may cause incorrect operation of the circuit.

Conventional glitch-free clock multiplexers assume that both clock signals are always running. However, in many low-power systems, one of the clocks may stop to save power. The circuit proposed in the referenced paper is designed to handle this situation by using timers to monitor the activity of the clock sources. When the selected clock stops, the timer detects the inactive clock and generates a disable signal. This allows the currently selected clock to be disabled and the other clock to be activated safely. The proposed multiplexer can therefore perform glitch-free switching even when the currently selected clock is not continuously running.

This type of circuit is useful in SoCs, embedded systems, and other digital designs where reliable clock switching is important for correct system operation.

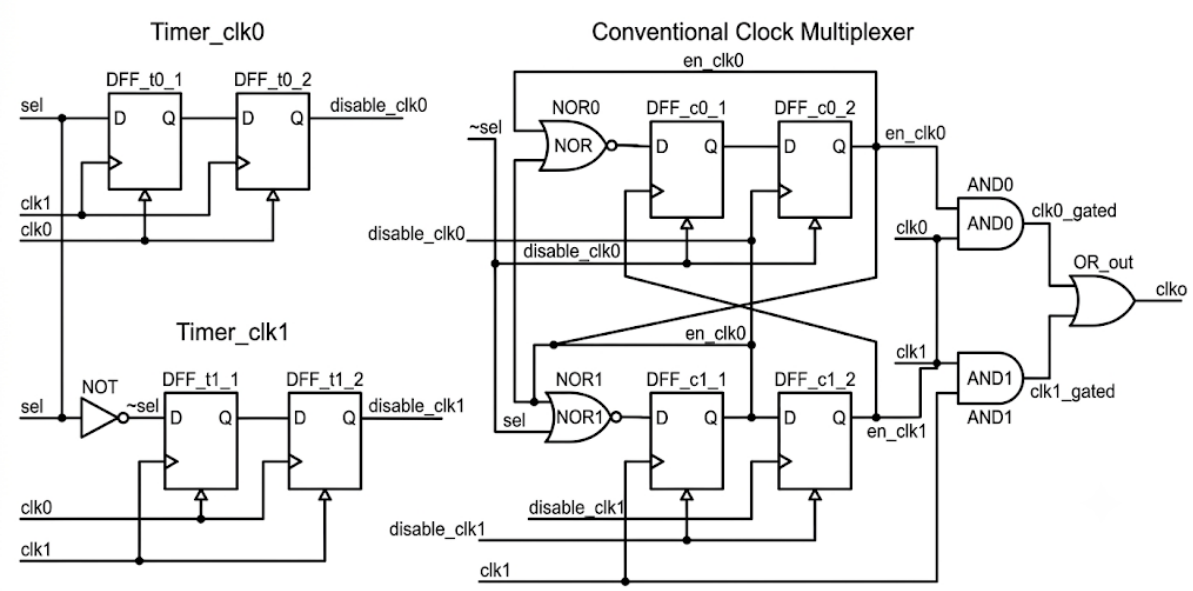
Reason to reproduce with eSim : This circuit is a good candidate for reproduction because it solves a practical problem found in modern digital systems. Implementing it in eSim will provide an open-source version of the design that can be easily studied, simulated, and verified by students and researchers. It will also help demonstrate that advanced clock management circuits can be reproduced using an open-source EDA tool.

Expected Outcome/outputs : The expected outcome of this research proposal is a working simulation of the proposed glitch-free clock multiplexer on eSim. The circuit should correctly select either of the two input clocks and switch between them without producing unwanted glitches or runt pulses.

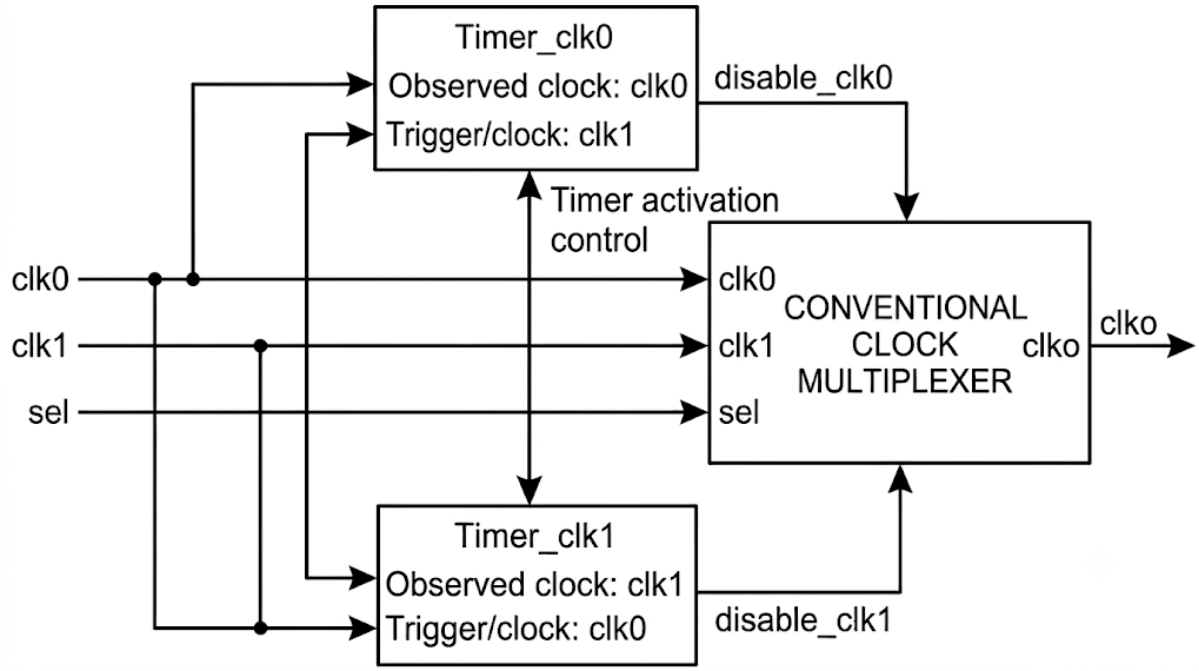
The simulation should also demonstrate the main feature of the proposed design in the reference paper, switching from the currently selected clock to the other clock even when

the selected clock has stopped running. The output clock should become active from the newly selected clock after the required switching delay.

Circuit Diagram(s) :



Block Diagram(s):



Expected Results (Input, Output waveforms and/or Multimeter readings):

The simulation will use two clock signals, clk0 and clk1, and a selection signal sel. clk0 and clk1 will be periodic digital clock waveforms with logic levels of approximately 0 V to 1.2 V. The sel will be a

digital signal with 0 V and 1.2 V levels used to select the clock. The disable_clk0 and disable_clk1 are expected to remain LOW during normal operation and become HIGH when the corresponding clock is detected as inactive. The output clk_o is expected to follow the selected clock without unwanted or short pulses during switching. When the selected clock stops, the timer is expected to detect the inactivity and allow the other clock to be selected after the required delay. The waveforms of clk0, clk1, sel, disable_clk0, disable_clk1, and clk_o will be observed to verify correct and glitch-free switching.

Research Paper/Journal/etc.

Title : A Glitch-free Clock Multiplexer for Non-Continuously Running Clocks
Pages: 11-15
Author : Steffen Zeidler, Oliver Schrape, Anselm Breitenreiter, Miloš Krstić
Link : https://ieeexplore.ieee.org/document/9217816

Source/Reference(s) :

[1] Steffen Zeidler, Oliver Schrape, Anselm Breitenreiter, Miloš Krstić, *A Glitch-free Clock Multiplexer for Non-Continuously Running Clocks*, 2020 23rd Euromicro Conference on Digital System Design (DSD).

[2] Clifford E. Cummings, *Clock Domain Crossing (CDC) Design & Verification Techniques Using SystemVerilog*, SNUG Boston, 2008.

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.