Title of the circuit: Design of a Two-Bit Magnitude Comparator Based on Pass Transistor, Transmission Gate and Conventional Static CMOS Logic Using esim

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Problem Statement : To Design an simulation model circuit for a Two-Bit Magnitude Comparator using Pass Transistor Logic, Transmission Gate Logic, and Conventional Static CMOS Logic. With the help of eSim, students can explore the design, functionality and performance of the comparator circuits

Theory/Description :

This study focuses on designing and simulating a Two-Bit Magnitude Comparator using eSim, leveraging Pass Transistor Logic (PTL), Transmission Gate Logic (TGL), and Conventional Static CMOS Logic (C-CMOS). The comparator compares two binary numbers and generates outputs indicating whether one is greater than, less than, or equal to the other.There are totally 3 circuits designed using esim (AGB,ALB,AEB) for simulating the 3 functionality of 2-bit magnitude comparator

Circuit Diagram(s) :

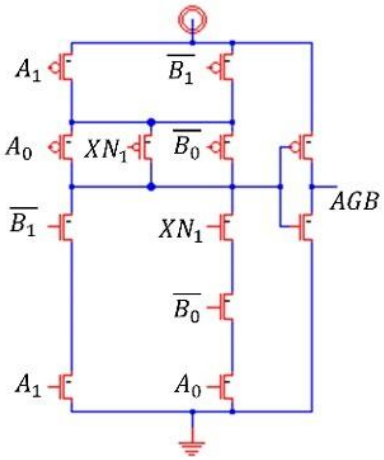

FIG-1:-Circuit of AGB(A greater than B)

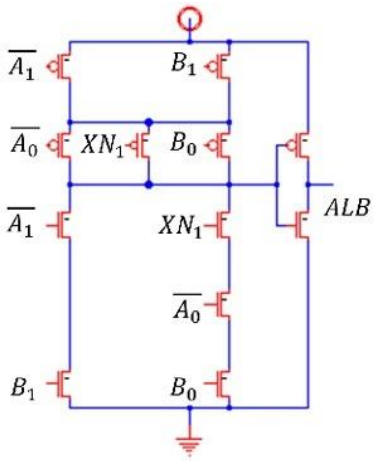

FIG-2:-Circuit of ALB(A less than B)

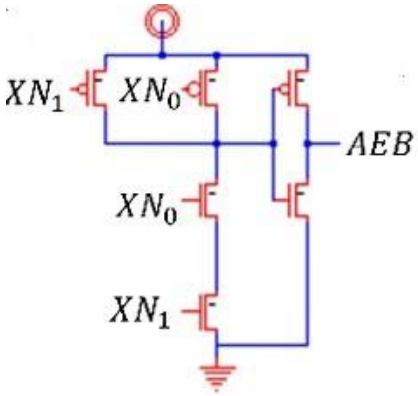

FIG-3:-Circuit of AEB(A equal to B)

SOURCES/REFERENCES:

- **Title of the paper :** Design of a Two-Bit Magnitude Comparator Based on Pass Transistor, Transmission Gate and Conventional Static CMOS Logic
- **Name of the journal/publication** : 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT)
- **Author(s):**Samiha Lubaba; K. M. Faisal; Moumita Sadia Islam; Mehedi Hasan (North south University,Bangladesh)
- **Chapter volume pages :**ICCCNT ISSN — 2020, Pages 1–5, Year 2020
- **Link:** https://ieeexplore.ieee.org/document/9225501