Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : A DTMOS-Based Memristor Emulator Circuit for Low-Power Biomedical Signal Conditioning

Theory/Description : A memristor is a passive two-terminal element whose resistance depends on the history of charge and flux through it. Physical memristors are not yet available in standard CMOS foundry processes, so memristor emulators built from ordinary transistors are used instead to study memristive behaviour and to build adaptive analog circuits such as self tuning filters, chaotic oscillators and neuromorphic front-ends. The circuit under study is one of the most compact floating memristor emulators reported to date. It uses only two Dynamic-Threshold MOS (DTMOS) transistors — one PMOS (Mp) and one NMOS (Mn) — and a single capacitor C, with no external DC bias and no static power draw. In a DTMOS device the body (bulk) terminal is tied to its own gate, so the transistor's threshold voltage shifts dynamically with the gate potential through the body effect.

Reason to reproduce with eSim :

1. Minimal transistor count (2 MOSFETs + 1 capacitor) makes this one of the simplest circuits in the memristor-emulator literature to reproduce in ngspice/eSim without needing a foundry-specific PDK.
2. Zero static power and no bias source simplifies the testbench compared to OTA- or multiplier-based emulators, which typically need multiple supply rails. • Cross-checked against the current FOSSEE Research Migration directory (254 entries as of Aug 2026) — no memristor-related circuit has been submitted, so this adds a new circuit class (adaptive / neuromorphic elements) to the open resource database.
3. Educational value: memristors are usually taught only in theory; a minimal, SPICE simulatable emulator lets students directly observe pinched hysteresis, frequency dependent memductance, and state retention. • Verifiable outcome: the source paper reports specific, checkable signatures (hysteresis pinching at the origin, lobe narrowing with frequency, near-zero static power) that can be directly compared against eSim results.

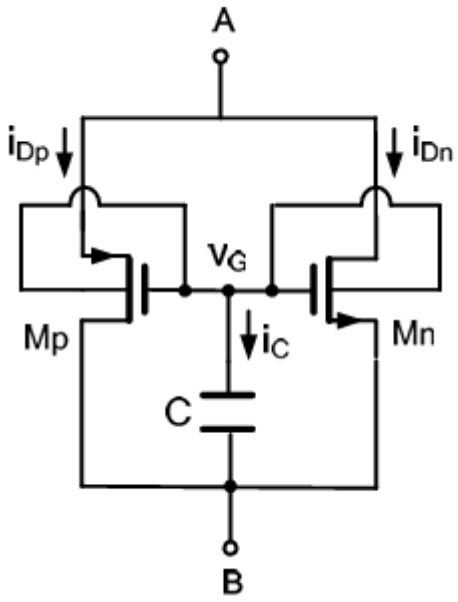
Expected Outcome/outputs :

• Pinched hysteresis loop: the iAB vs vAB plot should form a lens/figure-eight shape that pinches through the origin (i = 0 whenever v = 0) — the memristor fingerprint.

• Frequency dependence: sweeping the input frequency should widen the loop at low frequency and narrow it toward a straight line at high frequency.

• Capacitance tunability: increasing C should shift the narrowing frequency downward. • Near-zero static power at vAB = 0 (quiescent DC operating point)

Circuit Diagram(s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :

• Input: sinusoidal voltage source across A-B, amplitude 1.8 V peak (paper's exact drive level), swept across several decades of frequency.

• Output: transient $vAB(t)$ and $iAB(t)$ waveforms, and the derived $iAB - vAB$ hysteresis plot at each frequency.

• Multimeter / DC reading: near-zero quiescent current at vAB = 0, confirming zero static power operation.

• Validation criterion: loop area (hysteresis width) should decrease monotonically with increasing frequency, and the loop should always pass through the origin.

Concrete benchmark values reported in the paper (targets to validate the eSim build against):

Metric	Reported value
Simulated PHL frequency range	100 kHz - 500 MHz (0.18 μm foundry model, C scaled 200 pF - 100 fF)
Experimental PHL range (CD4007 prototype)	100 Hz - 1.5 kHz (C = 1 μmF) and 100 kHz - 800 kHz (C = 500 nF)
Dynamic power @ 500 MHz	318 μW
Energy per cycle @ 100 kHz / @ 500 MHz	107.7 pJ / 6.36 pJ
Temperature robustness	$-25\ ^{\circ}C$ to 75 $^{\circ}C$, negligible PHL distortion
Process-corner robustness	FF / FS / SF / SS / TT all preserve pinched, symmetric PHL
Monte Carlo (200 runs)	All 200 iterations reproduce characteristic hysteresis

Research Paper / Journal Reference Title A DTMOS-Based Memristor Emulator Circuit for Low-Power Biomedical Signal Conditioning

Author Imen Barraj Journal Micromachines, 2026, Vol. 17, Issue 3, Article 328

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Source / Reference(s)

• Original DTMOS threshold-voltage modeling reference cited in the source paper (body effect equation) — see paper's reference list, item [21].

• eSim / ngspice documentation for MOSFET model setup and DTMOS-style gate-bulk tying.

• FOSSEE Research Migration Project guidelines: https://esim.fossee.in/research migration-projec

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.