Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Single Edge Nibble Transmission (SENT) Protocol Implementation in eSim

Theory/Description : Single Edge Nibble Transmission (SENT) is a one-way, point-to-point serial protocol (SAE J2716) used to send high-resolution sensor data to a controller (e.g. an ECU) with minimal wiring. It uses a three-wire interface (signal line, +5 V supply, ground) and encodes each 4-bit "nibble" of data in the time between successive falling edges of the signal. Each nibble is transmitted as a fixed-duration low pulse (≥5 clock ticks, typically) followed by a variable high pulse: the total interval (low+high) in clock ticks ranges from 12 to 27, corresponding to decimal values 0–15. A calibration pulse (56 ticks long) always begins each frame, letting the receiver measure the tick time and compensate for clock drift. A typical message ("fast channel") contains 6 data nibbles (e.g. two 12-bit sensor values), one CRC nibble, and one status nibble. For example, Allegro's documentation notes that after the 56-tick sync pulse, status/comm nibble and up to six data nibbles follow, each of which is 5 ticks low plus 7–22 ticks high (total 12–27). This digital framing enables very fine resolution (e.g. >10 bits) without expensive A/D converters, and the built-in CRC/status offers error checking. In summary, the SENT transmitter generates a series of precisely timed pulses (voltage swings) from the sensor data, and the receiver measures the intervals between falling edges to recover the original 4-bit values.

Reason to reproduce with eSim : Open-source and educational: eSim is a free, open-source SPICE-based circuit simulator with a KiCad schematic frontend. It allows drawing and simulating analog/digital mixed circuits without costly licenses (an alternative to PSpice/OrCAD). Using eSim makes the design accessible to students and researchers on any platform.

Verifiable results: SENT is an asynchronous pulse protocol that benefits from circuit-level SPICE validation (edge timing, voltage levels). eSim's Ngspice engine can accurately simulate the analog timing and allow post-processing (e.g. measuring tick intervals). This ensures the design meets SAE J2716 timing (e.g. <6.5 µs falling edge, <18 µs rising edge jitter).

Open libraries: Because SENT is well-documented (app notes, open specs) and involves standard components (timers, gates, RC filters), it can be fully implemented in eSim using

digital IC models and analog passives. Its open nature (e.g. Wikipedia, application notes) makes it easy to verify against reference material.

Expected Outcome/outputs :

When simulated, the SENT circuit should produce a train of pulses on the signal line whose falling-edge timings encode the transmitted data. The key expectations are: [1]

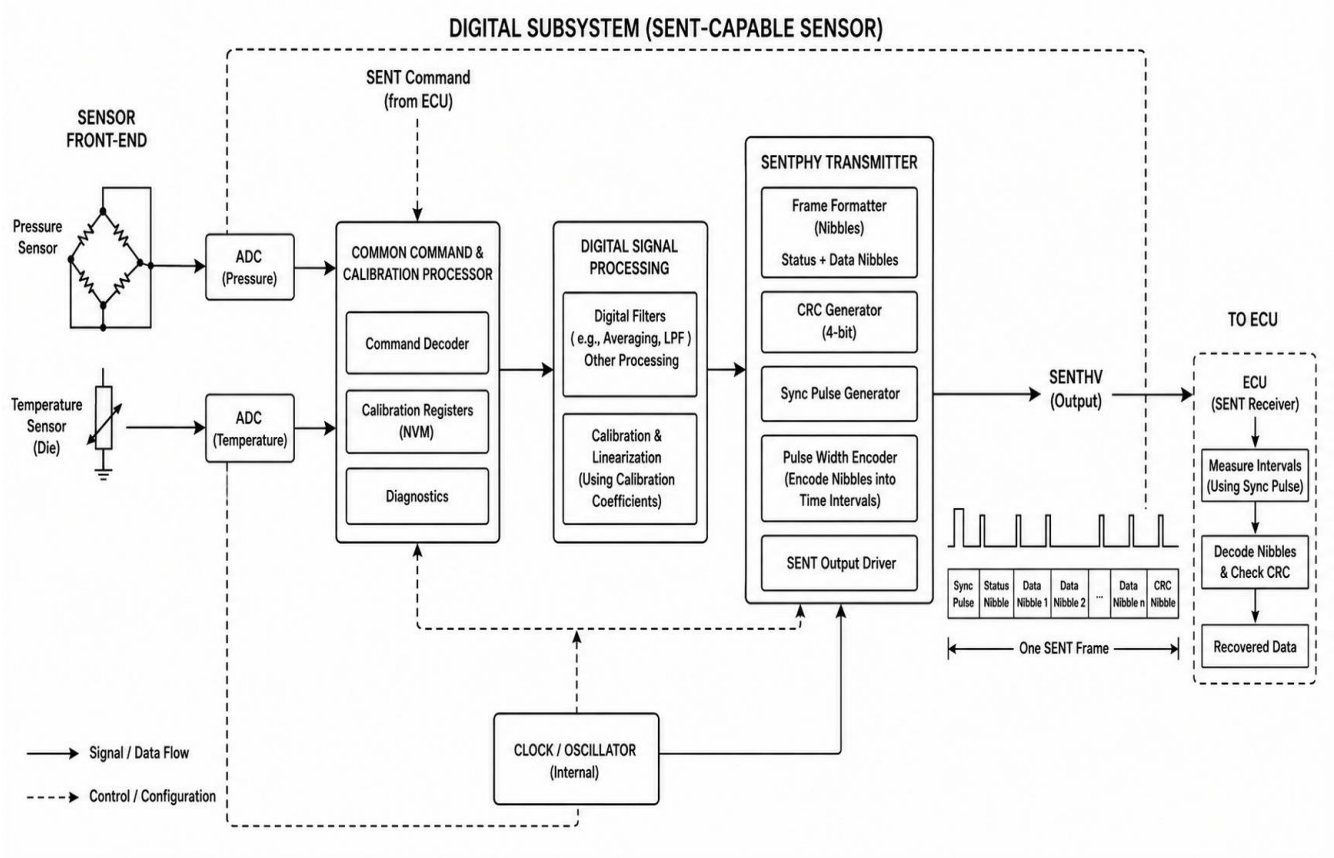
Correct pulse timing: The first falling edge should mark a calibration pulse about 56 ticks long. Each subsequent data nibble should appear as a 5-tick (or fixed) low level and a variable high level. For example, if a data nibble = 0 (decimal), the falling-edge interval will be 12 ticks; if nibble = 15, interval = 27 ticks. These intervals, as measured between falling edges, should exactly correspond to the sensor's raw data bits.

Voltage levels: The signal will swing from ground to ~5 V (with 0.5 V as low threshold and >4.1 V as high threshold as per the SAE spec). Multimeter readings on the pull-up node would show high ≈5 V and low ≈0 V states.

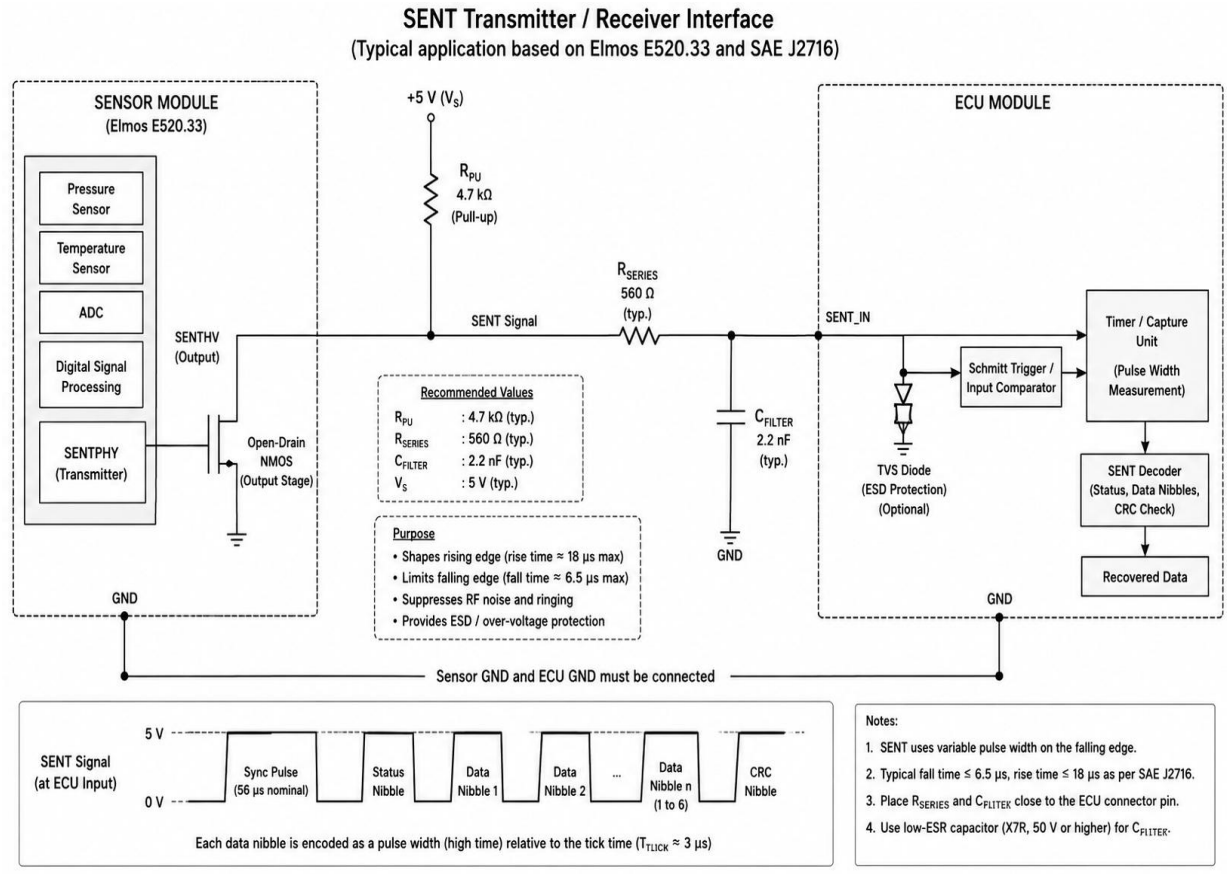
CRC/Status and Pause: After all data nibbles, the CRC nibble (4 bits) and an optional pause pulse will appear. The CRC nibble should match the computed CRC of the data (e.g. polynomial x^4+x^3+x^2+1). A correct design will show the CRC match expected values and any injected error should be detectable. The pause pulse (if used) will simply pad the frame to a fixed length.

Measured waveform: In summary, an oscilloscope plot of the output should match theory. For instance, one published simulation of a 6-nibble message (data=0x2A9C63) shows a total of 228 ticks (~1.824 ms). We would validate our circuit by observing the calibration pulse and data pulses on a scope (or Ngspice plot), verifying the tick counts correspond to the intended data.

Block Diagram (s) :



Circuit Diagram(s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) : When the simulation is run with a given sensor value, the output waveform on the SENT line should match the theoretical pattern. For example, if the sensor encoder outputs 24 bits of data (six 4-bit nibbles) plus CRC, the waveform will start with a 56-tick low pulse, followed by a sequence of low-high pulses. The low portion will always be ~5 ticks; the high portion's extra ticks encode each nibble (e.g. nibble 0→7 extra ticks for 12 total, nibble 15→22 extra for 27 total). In practice, one verifies by measuring time intervals: the distance (in simulation time) between falling edges should equal TICKS×t_tick for each nibble. In a sample simulation (data = 0x2A9C63, CRC=0xB) the total message took 228 ticks (≈1.824 ms), exactly as expected. We would check that our eSim voltage waveform shows the calibration pulse and all data pulses at the correct durations. For validation, we might decode the pulses back into nibble values (programmatically or by inspection) to confirm the original data and CRC are recovered. Any deviations (e.g. due to component tolerances or clock jitter) should be within the protocol's allowances.

Research Paper/Journal/etc. :

1)Title : J2716 SENT – Single Edge Nibble Transmission, Updates and Status
Author : Mark Costin, Robert Horner, Johannes Jaegers, Dirk Daecke, Alex Grossmann, Bernhard Opitz, Machiel ten Brinke, Tim Tiek, Eric Visser
Page No. : N/A (SAE Technical Paper No. 2011-01-1034)
Link : https://saemobilus.sae.org/papers/j2716-sent-single-edge-nibble-transmission-updates-status-2011-01-1034?

2)Title : Design and Implementation of Automotive SENT Interface
Author : Jong-Bae Lee, Seongsoo Lee
Page No. : Vol. 21, No. 3, pp. 256–259 (2017)
Link : https://www.kci.go.kr/kciportal/landing/article.kci?arti_id=ART002271356&

Source/Reference(s) :

M. Costin, R. Horner, J. Jaegers, D. Daecke, A. Grossmann, B. Opitz, M. ten Brinke, T. Tiek, and E. Visser, *"J2716 SENT – Single Edge Nibble Transmission, Updates and Status,"* SAE Technical Paper 2011-01-1034, SAE World Congress, Detroit, MI, USA, Apr. 2011.

J.-B. Lee and S. Lee, *"Design and Implementation of Automotive SENT Interface," Journal of the Institute of Electronics and Information Engineers (IEIE)*, vol. 54, no. 8, pp. 256–259, Aug. 2017.

E. Muzammal, S. Rajjarwal, M. C. Kim, and G. S. Byun, *"Analysis and Design of CRC-Based SENT Interface for Future Automotive Applications,"* in *Proc. International Conference on Information Networking (ICOIN)*, 2018.

F. Chen and R. Xia, *"Design of SENT Signal Acquisition System Based on LabVIEW," AIP Advances*, vol. 13, no. 10, Art. no. 105220, 2023.
