Research Migration Project

https://esim.fossee.in/research-migration-project

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Title of the circuit : Design and Simulation of Precharge-Free Content-Addressable Memory (PCAM) Cell.

Theory/Description : Content-Addressable Memory (CAM) is a specialized associative memory that simultaneously searches its entire array for a data word to return the matching address. Conventional CAMs use a dynamic two-phase clock (Precharge and Evaluation). Standard NOR-CAMs are fast but highly power-consumptive, while NAND-CAMs are low-power but slow and prone to charge-sharing. This project migrates a novel 2024 Precharge-Free CAM (PCAM) architecture. By using static XNOR logic to drive complementary transistors, PCAM completely eliminates the precharge phase. The N-PCAM variant uses NMOS pass-transistors for ultra-low energy, while the TG-PCAM variant uses Transmission Gates for high-speed, full-swing evaluation.

Reason to reproduce with eSim : The original 2024 research utilized proprietary Cadence Virtuoso tools at 65nm. Migrating this to eSim democratizes access to advanced VLSI memory design. Ngspice's transient analysis engine is fully equipped to precisely verify the nanosecond timing, logic thresholds, and energy consumption (via supply current integration) of these static architectures, creating a highly valuable open-source educational resource.

Expected Outcome/outputs : Simulated in eSim using standard Predictive Technology Models (PTM), the expected outcomes are:

1. Functional Verification: Transient waveforms demonstrating accurate "Match" and "Mismatch" states based on Search-Line (SL) inputs.
2. Precharge Elimination: Proof that PCAM cells perform continuous static evaluation without a clock-driven precharge signal.
3. Performance Validation: Delay measurements proving TG-PCAM achieves significantly faster search speeds than conventional NAND-CAMs.
4. Energy Validation: Supply current integration proving N-PCAM consumes drastically less energy per search than the NOR-CAM baseline.

Circuit Diagram(s) :

1. Baseline CAM cells

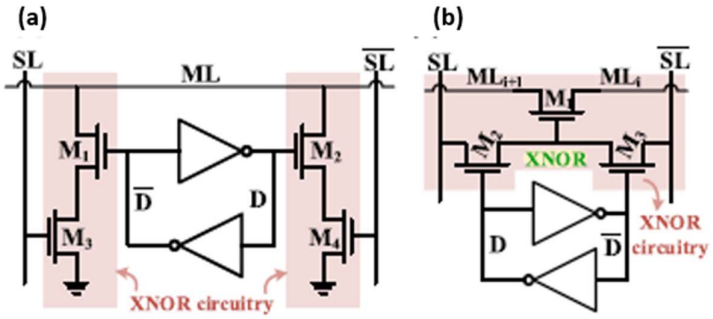


Figure 1. (a) NOR CAM cell and (b) NAND CAM cell

2. Proposed PCAM cells

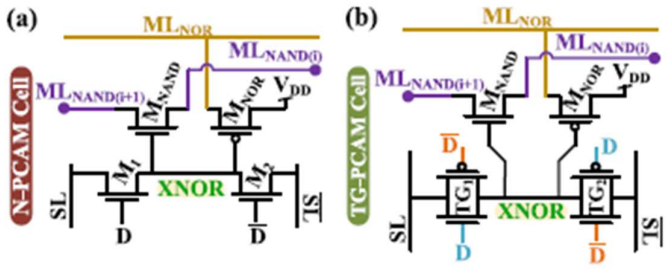
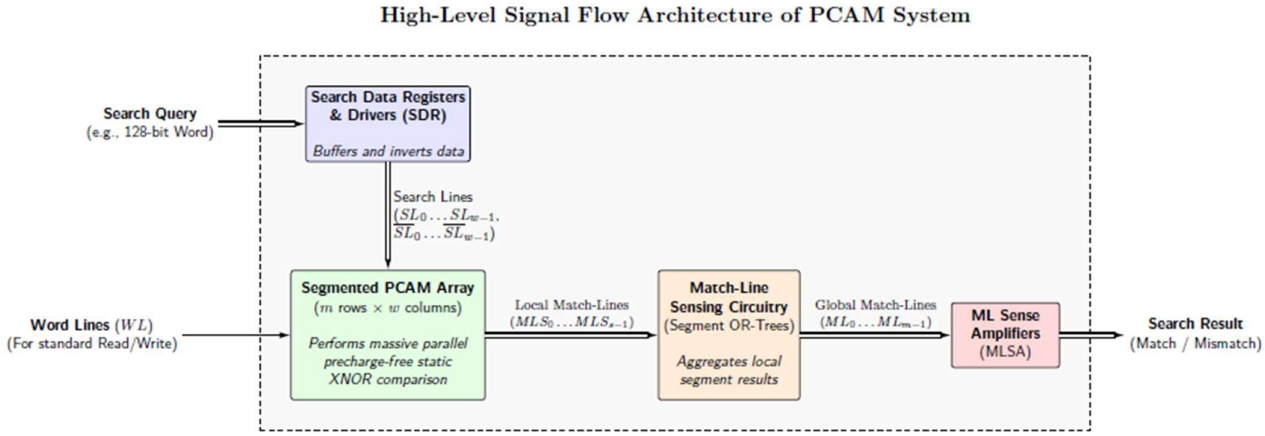


Figure 2. (a) N-PCAM and (b) TG-PCAM cells

Block Diagram :



Expected Results :

1. **Waveform Comparison (Precharge vs. Precharge-Free): Transient simulations will contrast baseline NOR/NAND CAMs (which require a mandatory, power-consuming precharge phase) against N-PCAM and TG-PCAM (which operate continuously and statically without a precharge clock).**
2. **Match/Mismatch States: During a "Match," waveforms will show the XNOR node driving the M_{NAND} transistor to discharge the Match-Line to 0 V. During a "Mismatch," the M_{NOR} transistor will aggressively charge the Match-Line to V_{DD} 1.2 V.**

Research Paper :

Title : Designing Precharge-Free Energy-Efficient Content-Addressable Memories

Author : Ramiro Taco, Esteban Garzón, Robert Hanhan, Adam Teman, Leonid Yavits, and Marco Lanuzza

Page No. : 2303–2314

Link : https://ieeexplore.ieee.org/abstract/document/10723100/
