



Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : SANA

Affiliation / Institution : Department of Electronics and Communication Engineering ,BVRIT HYDERABAD college of Engineering for Women, Hyderabad, Telangana.

Title of the circuit : Design and Simulation of a 3-Stage CMOS Ring Oscillator Using eSim

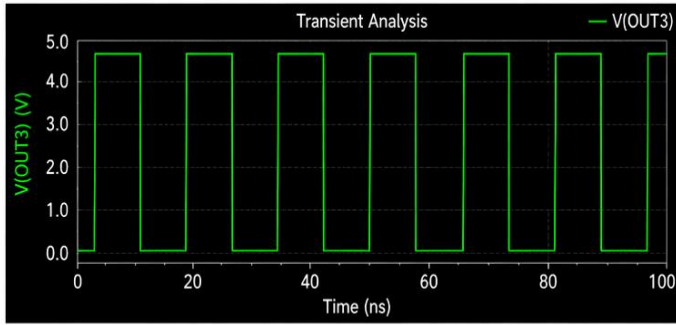
Theory/Description: The A **3-stage CMOS ring oscillator** is a circuit that generates a continuous oscillating signal without requiring an external clock source. It is built by connecting three CMOS inverter stages in a closed loop, where the output of the last stage is fed back to the first stage. Since the number of inverters is odd, the circuit cannot remain in a stable state and continuously switches between logic HIGH and LOW, producing oscillations. Each CMOS inverter consists of one PMOS and one NMOS transistor. The PMOS transistor pulls the output to logic HIGH, while the NMOS transistor pulls it to logic LOW. The oscillation occurs because of the propagation delay in each inverter stage. This delay causes the signal transitions to circulate through the loop, creating a periodic waveform. The oscillation frequency depends on the number of stages and the propagation delay of the inverters, given by:

$$f = 1/2Nt_p$$

Reason to reproduce with eSim : This project is reproduced using **eSim** because it provides a practical and cost-effective platform for designing and simulating CMOS circuits without requiring physical hardware. eSim supports transient analysis, allowing observation of waveform generation and timing behavior of the ring oscillator. It also enables easy modification of circuit parameters for performance evaluation, helping to verify theoretical concepts and gain hands-on experience in VLSI-oriented circuit design and simulation.

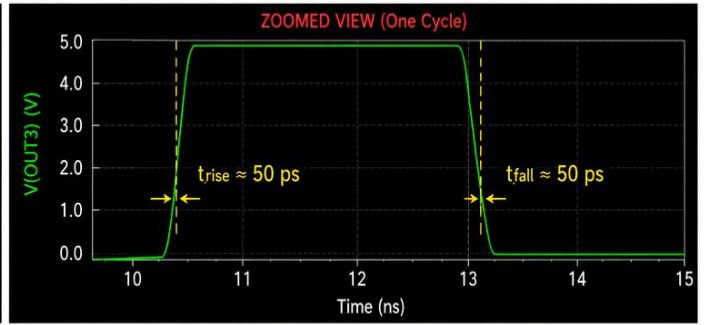
Expected Outcome/outputs: The expected outcome of this project is the successful design and simulation of a 3-stage CMOS ring oscillator in **eSim**, producing a continuous oscillating waveform without any external clock source. The output should demonstrate periodic switching between logic HIGH and LOW levels, confirming proper inverter operation and feedback loop functionality. The project also aims to analyze the oscillator's frequency, transient response, and timing characteristics, providing practical understanding of CMOS circuit behavior and VLSI design principles.

SIMULATION OUTPUT WAVEFORMS (NGSPICE)



From the waveform:

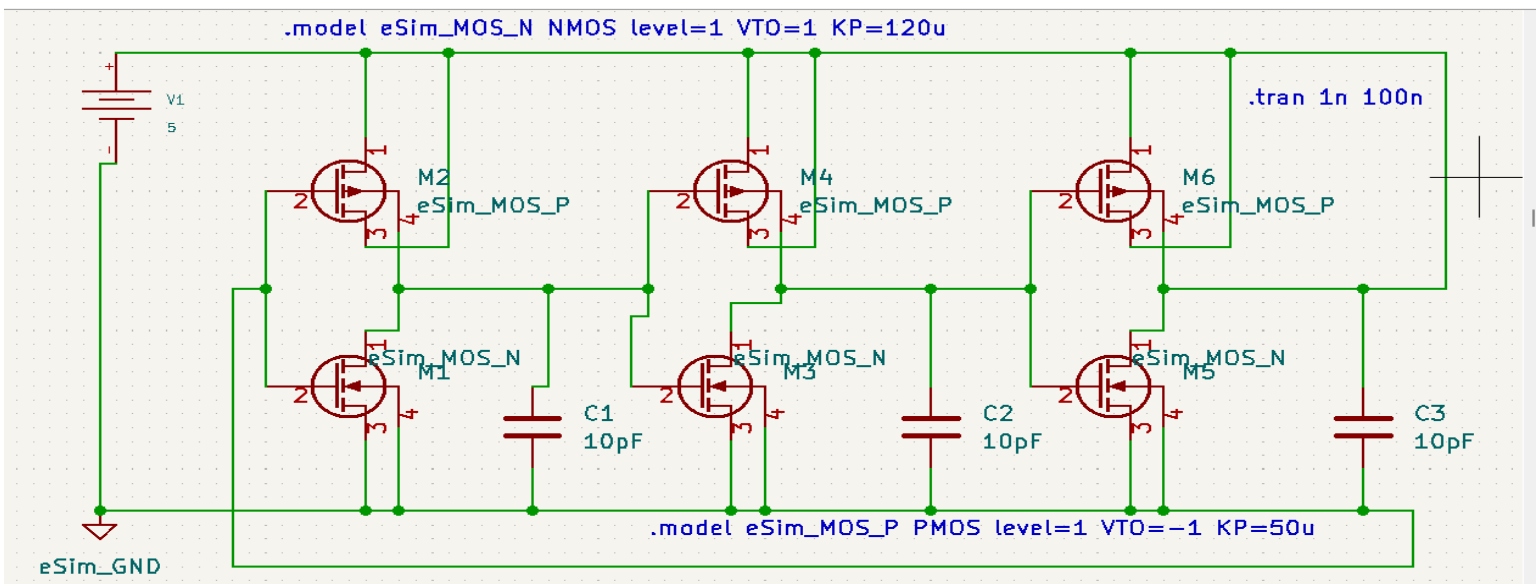
- Time Period (T) ≈ 10 ns
- Frequency (f) = $1 / T \approx 1 / 10$ ns = 100 MHz



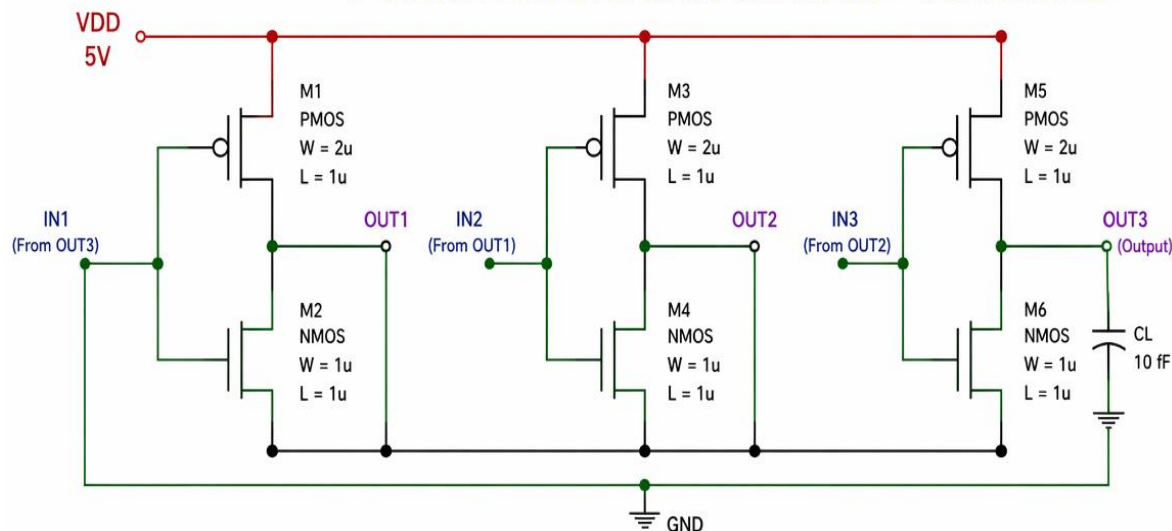
OBSERVATIONS

- A stable oscillation with nearly rail-to-rail output is observed.
- The output swings between ~ 0 V and ~ 5 V.
- Frequency ≈ 100 MHz (for given transistor sizes and load).

Circuit Diagram(s) : Circuit Diagram of 3-Stage CMOS Ring Oscillator (schematic)



3-STAGE CMOS RING OSCILLATOR – SCHEMATIC



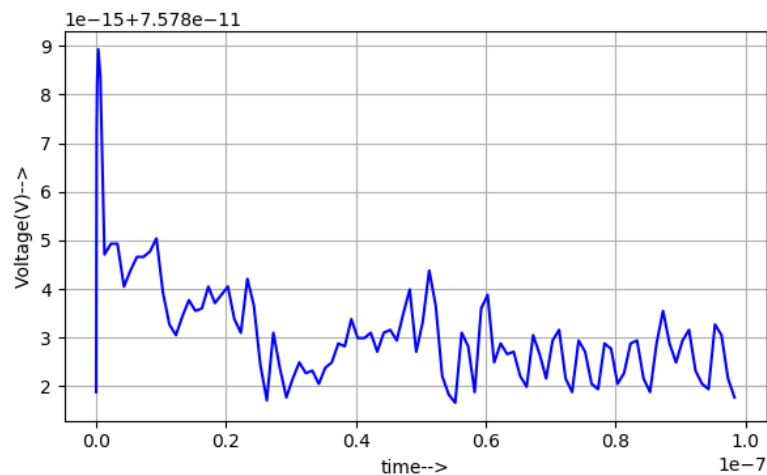
COMPONENT LIST

Component	Quantity
PMOS	3
NMOS	3
DC Voltage Source (VDD)	1
Capacitor (CL)	1
Ground	1
Voltage Probe	1

DESIGN PARAMETERS

- VDD = 5 V
- PMOS W/L = 2u / 1u
- NMOS W/L = 1u / 1u
- Load Capacitance CL = 10 fF
- Number of Stages = 3 (Odd)
- Technology = Generic 180 nm CMOS

Simulation Output :



Block Diagram (s) :

Single block showing:

- Input: Feedback from previous inverter stage
- Processing Block: 3-stage CMOS inverter chain (PMOS + NMOS transistors in each stage)
- Output: Continuous oscillating waveform

Expected Results (Input, Output waveforms and/or Multimeter readings) :

Input: No external clock input; only DC supply voltage (VDD = 5V)

- **Output:** Continuous oscillating waveform generated by feedback loop
- The simulation in **eSim** should produce periodic HIGH and LOW transitions, confirming ring oscillator operation.
- The waveform frequency depends on inverter delay and number of stages.
- Output should show a stable square-like oscillation without external triggering.

Research Paper/Journal/etc. :

Title: “Design and Analysis of CMOS Ring Oscillator for VLSI Applications”

- Author: Various VLSI researchers (general reference in CMOS oscillator studies)
- Page No.: 3–6
- Link: <https://ieeexplore.ieee.org/> (search: CMOS Ring Oscillator Design)

Source/Reference(s) :

- Weste, Neil H. E., and David Harris. *CMOS VLSI Design: A Circuits and Systems Perspective*. Pearson.
 - Rabaey, Jan M. *Digital Integrated Circuits: A Design Perspective*. Pearson.
 - Kang, Sung-Mo, and Yusuf Leblebici. *CMOS Digital Integrated Circuits*. McGraw-Hill.
 - eSim Documentation: <https://esim.fossee.in/resources>
 - Wikipedia: Ring Oscillator — https://en.wikipedia.org/wiki/Ring_oscillator
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