

Design and analysis of basic and Wilson current mirror in 180nm CMOS technology

Name of participant : **Abhijit Baral**

Education : **Btech in Electronics and Telecommunication Engineering (4th sem).**

University : **Veer Surendra Sai University of Technology, Burla**

Project guide : **Prof. Dr. Aditya Hota**

Problem statement : **Designs and analysis of Basic and Wilson Current Mirror circuits in 180nm technology**

Theory / Description : **Current mirrors are essential components in analog circuit design, enabling precise current replication and biasing. This project focuses on the design and simulation of a basic current mirror and a Wilson current mirror using 180nm CMOS technology. The circuits will be analyzed through DC, AC, and output impedance analysis using e-Sim 2.4. The original simulations in the research paper were performed in cadence virtuoso. We aim to compare the results to highlight discrepancies, if any, and validate the feasibility of using open-source tools in professional-grade analog design workflows.**

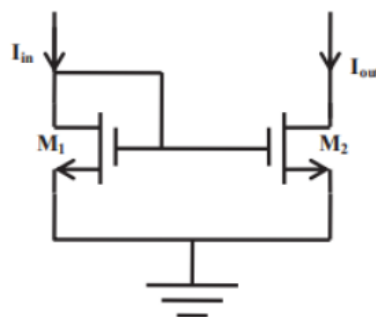


Fig.1 Basic current mirror

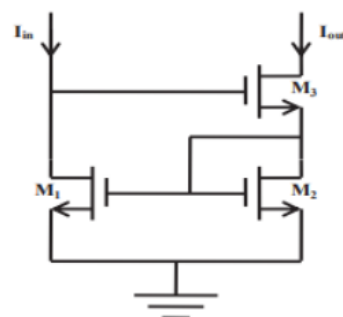


Fig.2 Wilson current mirror

Source / Reference(s) :

Title of the paper : **Design and Analysis of Basic AND Wilson Current Mirror in 45nm AND 180nm CMOS Technology**

Name of the journal : **Quest Journals. Journal of Electronics and Communication Engineering Research**

Chapter volume pages : **Volume 9 ~ Issue 9 (2023) pp: 39-49**

Link : <https://www.questjournals.org/jecer/papers/vol9-issue9/09093949.pdf>