Research Migration Project

https://esim.fossee.in/research-migration-project

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Affiliation / Institution : National Institute of Technology, Silchar

Title of the circuit : Design and Implementation of a 3-Tap FIR Filter using Basic Digital Logic in eSim

Theory/Description: A Finite Impulse Response (FIR) filter is a fundamental digital signal processing (DSP) component widely used for noise reduction and signal conditioning. FIR filters are inherently stable and exhibit linear phase characteristics due to the absence of feedback.

The output of an FIR filter is given by:

$$y[n] = h_0 x[n] + h_1 x[n-1] + h_2 x[n-2]$$

This project implements a **3-tap FIR filter** using a **Multiply-Accumulate (MAC) architecture** in eSim. The design is divided into three main functional blocks:

- **Delay Block:** Implemented using D Flip-Flops to generate delayed input samples $x[n-1]$and $x[n-2]$
- **Multiplier Block:** A 2-bit binary multiplier implemented using AND gates to generate partial products and Half Adders.
- **Adder Block:** Ripple Carry Adders (Full Adders) used to accumulate the products

The design follows the fundamental FIR architecture described in literature, where multipliers, adders, and delay elements form the core building blocks of the filter.

Reason to reproduce with eSim : The referenced paper implements an optimized FIR filter using advanced multiplier and adder architectures. In this work, a simplified version of the FIR filter is implemented using basic digital logic components in eSim to reproduce the fundamental architecture and verify its operation.

This project aims to reproduce the fundamental FIR filter architecture in eSim, an open-source simulation platform, with the following objectives:

- To understand FIR filter operation at gate-level hardware abstraction
- To provide an accessible and reproducible implementation using open-source tools
- To verify FIR functionality using ngspice simulation
- To demonstrate how complex DSP systems can be built using basic digital building blocks

This reproduction simplifies the optimized architecture presented in the paper while preserving the core operational principles.

Expected Outcome/outputs :

- Correct generation of 2- bit delayed signals $x[n-1]$, $x[n-2]$using D Flip-Flops.
- Accurate multiplication of 2-bit input samples with filter coefficients using binary multipliers to get 4-bit binary products.
- Proper accumulation of results using adders to produce final FIR output which will be 6-bit to handle overflowing.
- 6-bit output (5-bit and carry bit) representing filtered version of the input signal.
- Functional verification of the FIR filter through simulation.

Circuit Diagram(s) :

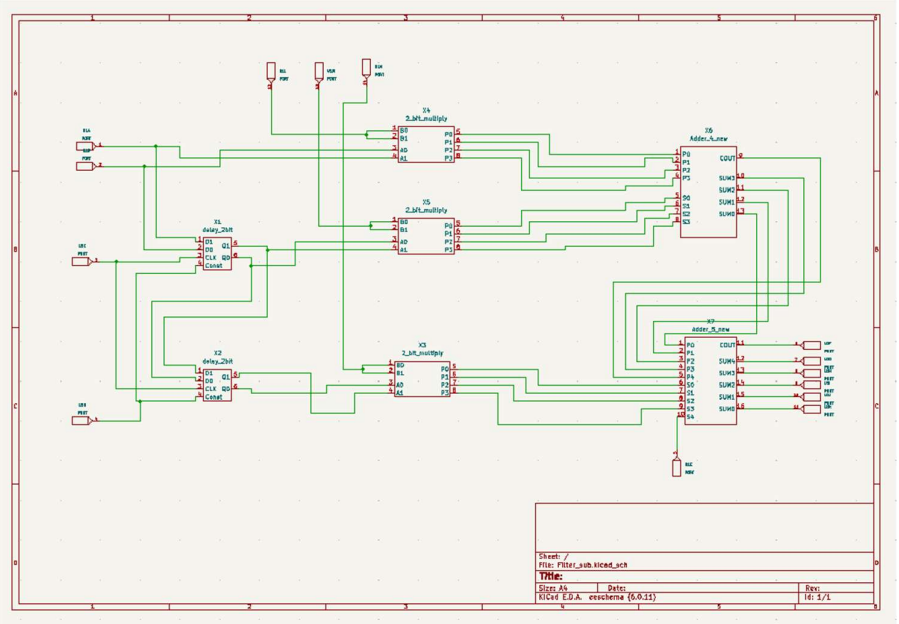

Fig 1: 3-tap FIR filter circuit implemented in eSim showing modular delay elements, multipliers, and adder blocks.

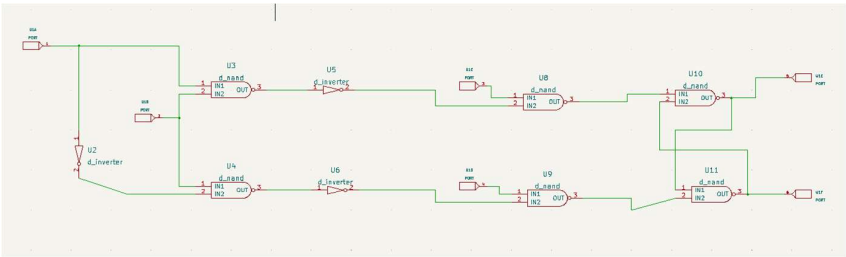

Fig 2: Gate-level implementation of D Flip-Flop using NAND gates and inverters, used as delay element in the FIR filter.

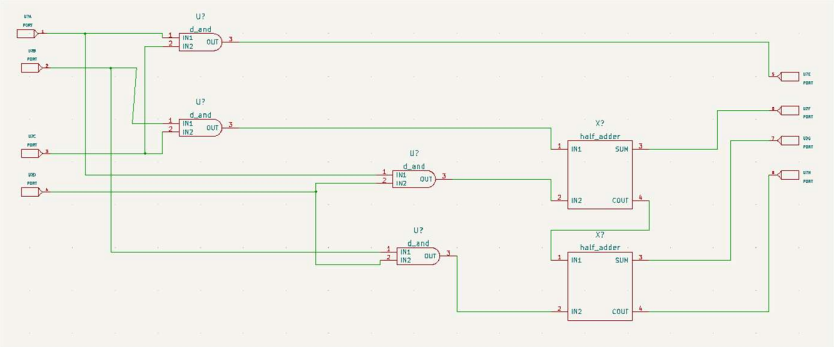

Fig 3: 2-bit binary multiplier implemented using AND gates and half adders for partial product generation and accumulation.

Block Diagram (s) :

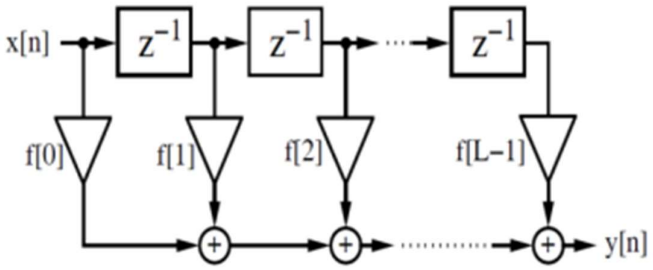

Fig: General FIR filter block diagram showing delay elements, multipliers, and adders. In this work, a 3-tap FIR filter is implemented using three delay stages and corresponding multiplier-adder blocks.

Expected Results (Input, Output waveforms and/or Multimeter readings) :

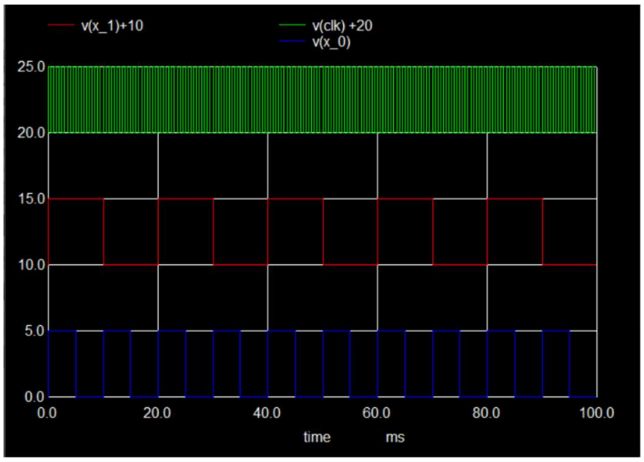

Fig 1: Clock and input signal x[1:0]

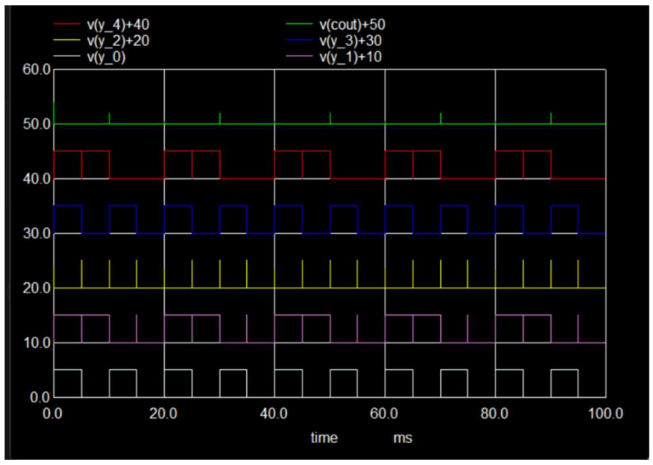

Fig 2: output 6 bits y[4:0] and cout

The waveforms demonstrate input, clock and output of the FIR filter. The output corresponds to the weighted sum of present and past input samples of the 3-tap FIR filter.

Research Paper/Journal/etc. :

Title : Design and Implementation of FIR Filter using Low Power and High-Speed Multiplier and Adders

Author : O. Venkata Krishna

Journal: CVR Journal of Science and Technology, 2019

Page No. : (Approx.) 80–84

Link :

https://www.researchgate.net/publication/330640108_Design_and_Implementation_of_FIR_Filter_usingLow_Power_and_High-Speed_Multiplier_and_Adders

Source/Reference(s) :

1) https://www.geeksforgeeks.org/electronics-engineering/difference-between-fir-filter-and-iir-filter/
2) https://analogcircuitdesign.com/FIR-filter/