Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : Subhadeep Bag

Affiliation / Institution :

Department of Electrical and Electronics Engineering, Rajiv Gandhi Institute of Petroleum Technology (RGIPT), Jais, Amethi, Uttar Pradesh, India.

Title of the circuit :

Transistor-Level Implementation and Simulation of CA3140 BiMOS Operational Amplifier

Theory/Description :

The circuit represents the transistor-level implementation and testing of the CA3140 BiMOS operational amplifier, which combines a MOSFET input stage with a bipolar transistor output stage to achieve high input impedance and high output drive capability.

The internal architecture consists of three main stages. The input stage uses a differential pair of PMOS transistors, providing extremely high input impedance and low input current. This stage converts the differential input signal into a single-ended signal. The second stage is a high-gain voltage amplifier that provides the majority of the voltage gain and includes internal frequency compensation for stability. The output stage is a class AB push-pull amplifier using bipolar transistors, enabling efficient current sourcing and sinking to drive low-impedance loads.

A biasing network and current mirrors ensure constant current operation across all stages, improving linearity and thermal stability. The amplifier is internally compensated, allowing stable operation in unity gain configurations.

In the test configuration (voltage follower), the output is directly fed back to the inverting input, resulting in unity gain and high bandwidth operation. The circuit demonstrates key dynamic characteristics such as slew rate, settling time, and bandwidth, as observed in the transient response waveforms.

Overall, the circuit operates as a high-performance operational amplifier suitable for applications such as active filters, signal conditioning, and voltage buffering.

Reason to reproduce with eSim :

This circuit is suitable for reproduction in eSim as it enables detailed transistor-level simulation of the CA3140 operational amplifier using an open-source platform. It provides strong educational value by allowing analysis of internal stages such as the differential input, gain stage, and output stage.

eSim simplifies circuit implementation and testing, making it easier to study key parameters like gain, slew rate, and transient response. It also allows verification of datasheet characteristics (such as those shown in the test circuit) without requiring physical hardware.

Overall, using eSim helps in understanding internal working, validating performance, and exploring design modifications efficiently.

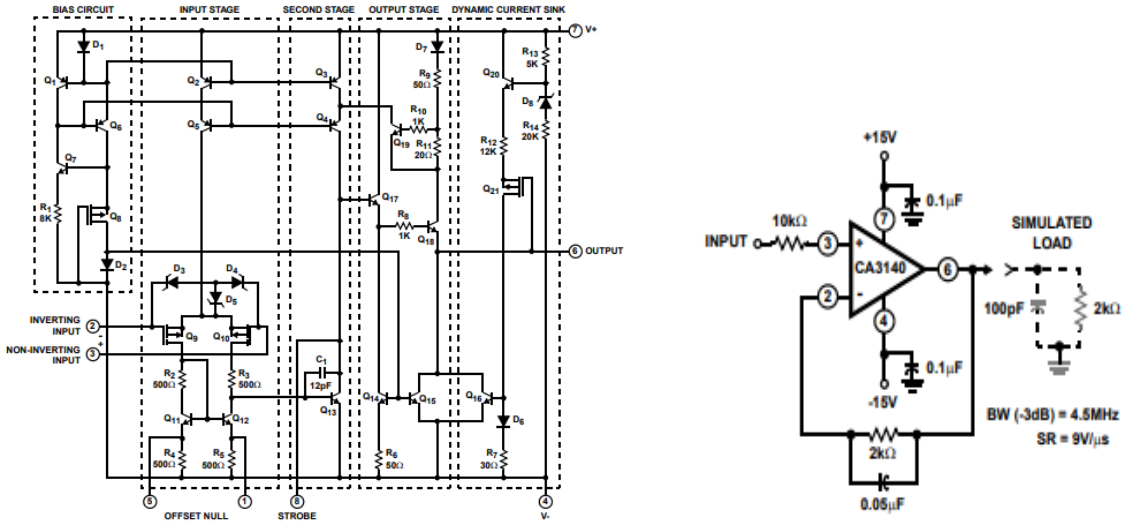
Expected Outcome/outputs :

When simulated in eSim, the circuit is expected to operate as a voltage follower, producing an output signal that closely tracks the input with unity gain. The output waveform should match the input waveform in shape, with minimal distortion and slight delay due to finite slew rate.

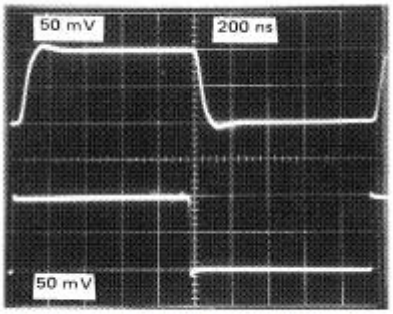
The simulation should demonstrate key performance parameters such as high input impedance, wide bandwidth, fast settling time, and slew rate (~9 V/µs). Transient analysis should show proper rise/fall behavior similar to the datasheets waveforms.

Performance can be validated by comparing the simulated output with the expected results from the test circuit, ensuring accurate signal tracking and stable operation.

Circuit Diagram(s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :



Top Trace: Output; 50mV/Div., 200ns/Div.
Bottom Trace: Input; 50mV/Div., 200ns/Div.

Research Paper/Journal/etc. :

Renesas Electronics Corporation, "CA3140, CA3140A – 4.5MHz BiMOS Operational Amplifier with MOSFET Input/Bipolar Output," Datasheet, July 2005.

Available: https://www.renesas.com/en/document/dst/ca3140-ca3140a-datasheet

Source/Reference(s) : Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGraw-Hill, 2nd Edition.
