Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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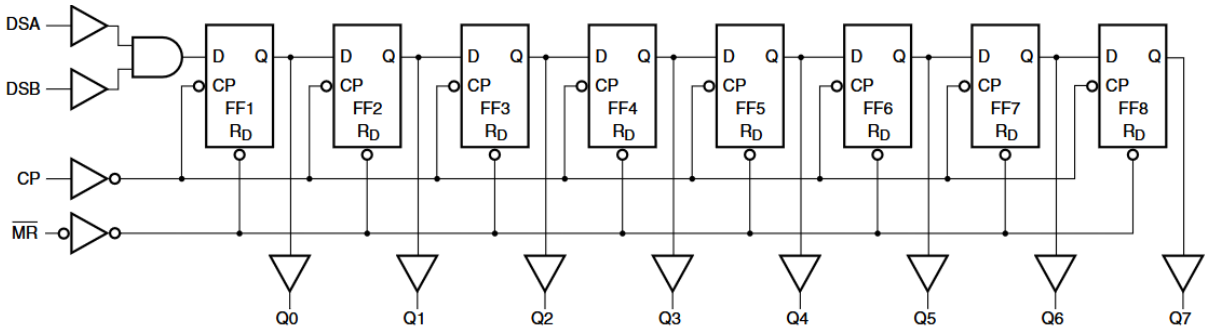
Title of the circuit : 8-bit serial-in, parallel-out (SIPO) shift register using D Flip-Flops

Theory/Description : This circuit is an 8-bit Serial-In Parallel-Out (SIPO) shift register implemented using cascaded D flip-flops. The serial input data is applied to the first flip-flop, and with each clock pulse, the data shifts sequentially through the chain of flip-flops. Each stage stores one bit, allowing the serial data stream to be converted into an 8-bit parallel output. The common clock ensures synchronized shifting, while the master reset initializes all outputs to zero. This configuration is widely used in digital systems for data storage, data transfer, and serial-to-parallel conversion in communication interfaces.

Reason to reproduce with eSim : This circuit is reproduced in eSim to verify the correct shifting behaviour, timing synchronization, and reset functionality before hardware implementation. Simulation helps visualize how each bit propagates through the flip-flops with every clock pulse and ensures accurate serial-to-parallel conversion. Using eSim simplifies debugging, reduces implementation errors, and provides a clear understanding of sequential circuit operation.

Expected Outcome/outputs : The simulated output should show serial data being shifted through the flip-flops with each clock pulse, eventually appearing as an 8-bit parallel output across Q0 to Q7. The outputs should update synchronously with the clock, and all outputs should reset to zero when the master reset is activated. This confirms correct data shifting, proper synchronization, and reliable operation of the SIPO shift register.

Circuit Diagram(s) :



INTERNAL CIRCUIT DIAGRAM OF 74HC164

Expected Results (Input, Output waveforms and/or Multimeter readings) : The input to the circuit consists of a serial digital data stream applied at the data input (DSA/DSB) along with a periodic clock pulse (CP). The clock waveform is a square wave, typically at a constant frequency, which controls the shifting operation of the register. The master reset (MR) signal, when activated, forces all outputs to logic LOW.

The output consists of eight parallel digital signals (Q0 to Q7). Each output represents one bit of the input data sequence, delayed by one clock cycle per stage. The waveforms at Q0 to Q7 appear as time-shifted versions of the input serial data, forming a staircase-like propagation across stages.

Research Paper/Journal/etc. :

1. 74HC164BQ Datasheet, *NXP Semiconductors*
   - Primary reference for internal logic structure, timing characteristics, and functional operation of the shift register.
2. M. Morris Mano, Digital Design, *Pearson Education*
   - Explains fundamental concepts of shift registers, sequential circuits, and serial-to-parallel data conversion.

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