Sample and Hold Circuit using OpAmp-741

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Abstract

A sample and hold circuit is a vital component in signal processing applications. This report presents the design and implementation of a sample and hold circuit using the LM741 operational amplifier and an NMOSFET. The circuit samples an input sine wave signal during the high state of a control pulse and holds the sampled value until the next sampling period. Key components include a sine wave generator, a control pulse for the MOSFET, and negative feedback to enhance stability. The expected output waveform is a discrete version of the input signal, held constant during each sampling interval.

Keywords: Sample and Hold, LM741, NMOSFET, Signal Processing, Negative Feedback

1 Introduction

The sample and hold circuit is an essential building block in analog-to-digital conversion and signal processing systems. It samples an analog input signal at specific intervals and holds the sampled value constant for a certain duration. This functionality is crucial for maintaining signal integrity during conversion or processing stages. The need for such a circuit arises from the requirement to process discrete-time signals in digital systems while preserving the characteristics of the original analog signal.

In this project, we have designed a sample and hold circuit using an LM741 operational amplifier and an NMOSFET. The circuit uses a control pulse to determine the sampling intervals and negative feedback to improve the stability and accuracy of the operation.

2 Purpose of the Circuit

The primary purpose of the sample and hold circuit is to:

- Sample an analog input signal at predefined intervals.
- Maintain or "hold" the sampled value for further processing.
- Provide a stable input to analog-to-digital converters (ADC) or other signal processing components.

This circuit is widely used in communication systems, instrumentation, and control applications.

3 Working of the Circuit

The circuit comprises the following key components:

- **Input Signal:** A sine wave generated by a function generator to act as the analog input.
- **Control Signal:** A pulse wave used to control the switching of the NMOSFET.
- **NMOSFET:** Acts as a switch to sample the input signal during the high state of the control pulse.
- **Operational Amplifier (LM741):** Configured with negative feedback to maintain stability and provide a buffered output.
- **Feedback Capacitor:** Holds the sampled voltage during the hold phase.

When the control pulse is high, the NMOSFET conducts, allowing the input signal to charge the holding capacitor. During the low state of the control pulse, the NMOSFET turns off, and the capacitor retains the sampled voltage. The operational amplifier buffers this voltage to provide a stable output.

4 Circuit Diagram

The circuit diagram is shown below:

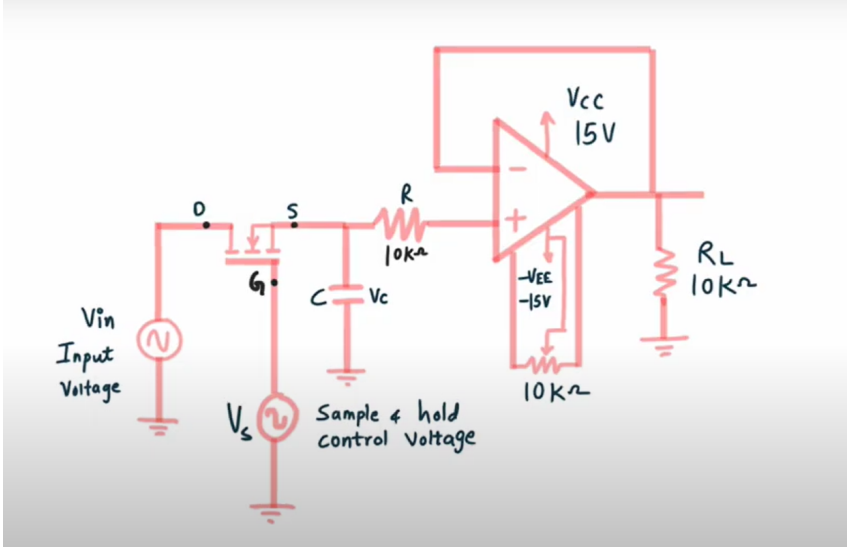

Figure 1: Sample and Hold Circuit Diagram

The NMOSFET in the circuit is configured in a **common-source configuration**, where the source is grounded, the gate is driven by the pulse signal, and the drain is connected to the sampling capacitor. This configuration allows the MOSFET to function effectively as a switch, with the gate voltage controlling its conduction state. The capacitor acts as the holding element, while the operational amplifier with negative feedback ensures signal buffering and stability.

5 Expected Waveform

The expected output waveform consists of discrete steps corresponding to the sampled values of the input sine wave. Each step represents the voltage held during the hold phase of the sampling period. The timing of the steps aligns with the high states of the control pulse.

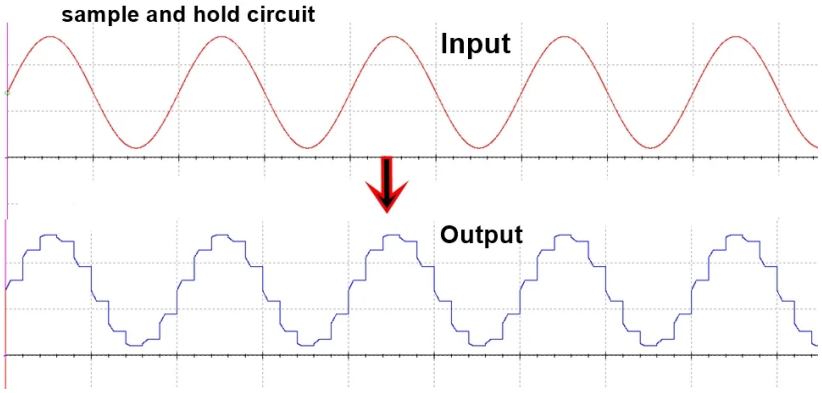

Figure 2: Expected Output Waveform

6 eSim Circuit

The eSim simulation of the circuit is depicted below:

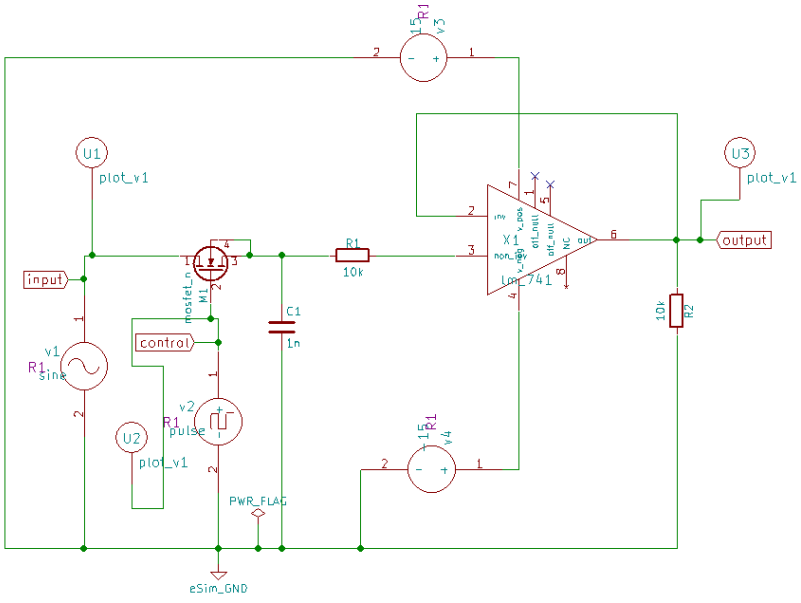

Figure 3: eSim Circuit Simulation for Sample and Hold Circuit

7 Output

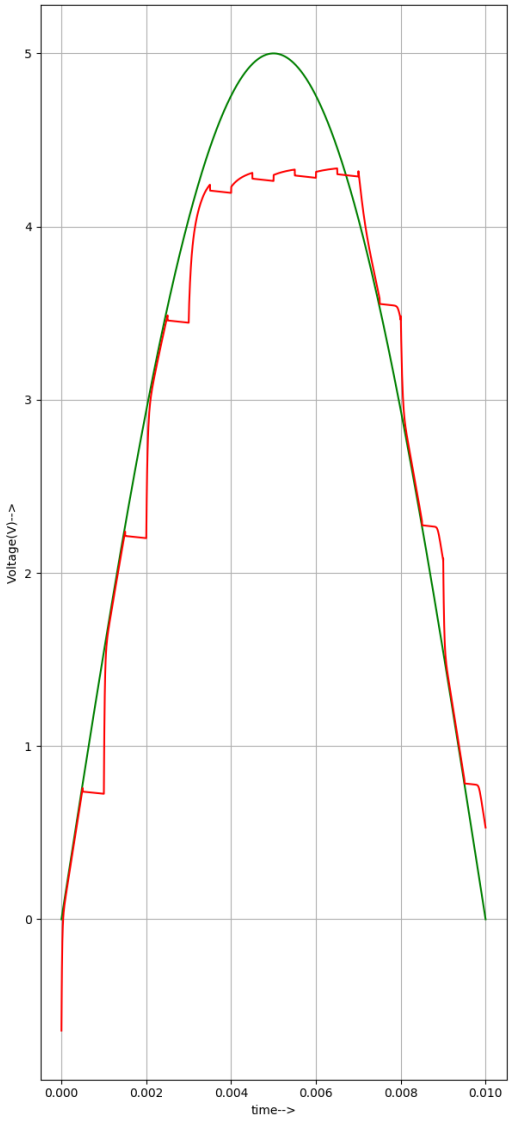

Figure 4: Simulated results

8 References

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