Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

FOSSEE Research Migration Project: Abstract

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Title of the Circuit: Design and Implementation of a Sinc3 Digital Filter

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Theory / Description

The Sinc3 (third-order cascaded integrator-comb) filter is a digital low-pass filter widely used as a decimation filter in Sigma-Delta Analog-to-Digital Converters. It functions by averaging the high-frequency bitstream from a modulator to produce high-resolution multi-bit samples at a lower rate. Structurally, it consists of three stages of integrators operating at a high sampling rate, followed by a decimator, and three stages of combs operating at the lower output rate. The transfer function in the z-domain is:

$$H(z) = \left(\frac{1 - z^{-N}}{1 - z^{-1}}\right)^3$$

where N is the decimation ratio. It is preferred for its hardware efficiency as it requires no multipliers, only adders and delays.

Reason to Reproduce with eSim

Migrating this design to eSim is highly beneficial because:

- Open-Source Validation: It demonstrates eSim's capability to handle mixed-signal or digital logic blocks (via Ngspice and GHDL/Verilog integration).
- Verification: It verifies that results from proprietary tools like MATLAB/Simulink or Xilinx Vivado can be accurately replicated in a free, open-source environment.

Expected Outcome / Outputs

The primary outcome is a functional simulation of the Sinc3 filter within eSim. The filter is expected to suppress high-frequency quantization noise from a pulse-density modulated

(PDM) input. We expect to see a smooth, decimated digital output that tracks the low-frequency components of the original signal.

Circuit Diagram(s)

(Note: You will need to attach your eSim Schematic here. It should show the interconnection of the Flip-flops, Adders, and the Decimation Clock logic.)

Block Diagram(s)

The system architecture follows a linear pipeline:

[Input Bitstream]→ [3x Integrator Stages]→ [Downsampler (1/N)]→

[3x Comb Stages] → [Digital Output]

Expected Results

- Input: A 1-bit high-frequency PDM (Pulse Density Modulation) signal or a fast-switching square wave representing noise-shaped data.
- Output Waveform: A stepped multi-bit digital waveform. When filtered, this should resemble a clean sine wave (if the original modulator input was a sine wave).
- Frequency Response: A "Sinc" shaped magnitude response with deep nulls at multiples of the decimation frequency.

Research Paper / Journal / etc:

- Title: **An optimized two stages low power sinc3 filter for ΣΔ modulators**
- Author: A. Lombardi; P. Malcovati; A. Basto; E. Bonizzoni; F. Maloberti
- Link: https://ieeexplore.ieee.org/document/4401816
- Source / Reference(s)

1. Hogenauer, E., "An economical class of digital filters for decimation and interpolation," IEEE Transactions on Acoustics, Speech, and Signal Processing.
2. eSim User Manual, FOSSEE, IIT Bombay.