

Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and Simulation of Dynamic CMOS Domino Logic Circuits (AND, OR, NAND and NOR) using eSim

Theory:

Dynamic CMOS domino logic is a high-speed digital logic design technique widely used in VLSI systems. It operates in two phases: precharge and evaluation. During the precharge phase, the dynamic node is charged to the supply voltage (VDD), and during the evaluation phase, the node may discharge depending on the input conditions through an NMOS pull-down network.

In this project, domino implementations of AND, OR, NAND and NOR gates are designed using CMOS technology. Each circuit consists of a precharge PMOS transistor, an evaluation NMOS network, a keeper PMOS transistor to maintain charge, and a CMOS inverter for output restoration. The circuits demonstrate reduced propagation delay and improved switching speed compared to static CMOS logic.

Reason to reproduce with eSim :

- eSim provides an open-source platform for simulating advanced VLSI circuits.
- Dynamic domino logic circuits are not commonly available in standard eSim examples.
- Helps in understanding real-world high-speed CMOS design techniques.
- Enables verification of timing behavior, charge sharing effects, and leakage issues.
- Useful for academic learning and research-level circuit analysis.

Circuit Diagram(s) :

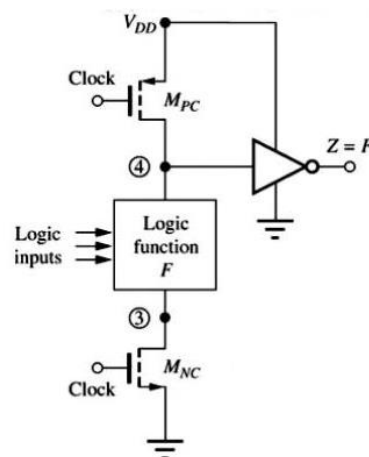


Figure 1. A Domino Logic Circuit

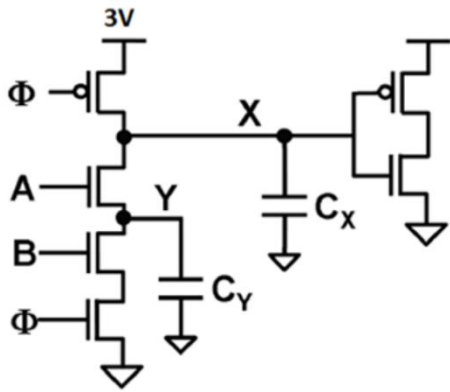


Figure 2. Domino style dynamic logic NAND gate

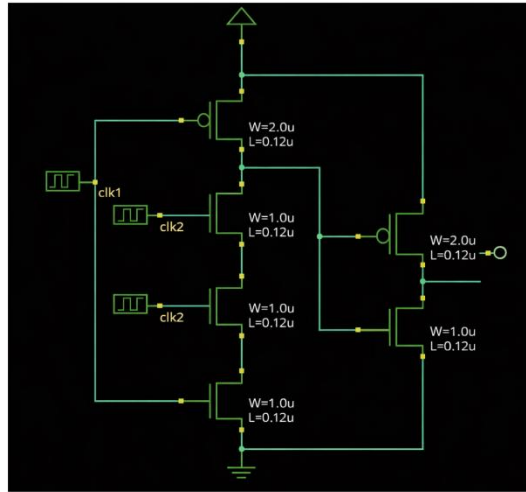


Figure 3. Dynamic logic AND gate

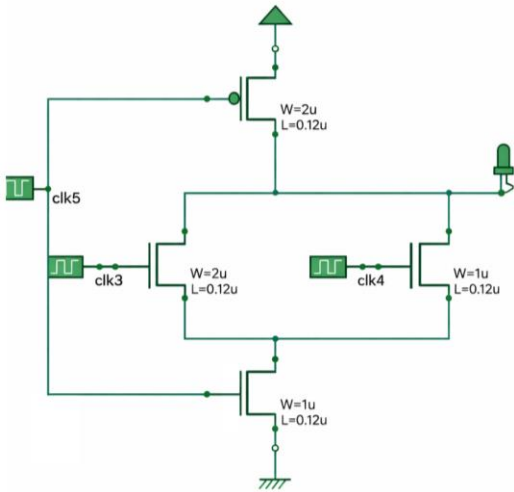


Figure 4. Dynamic logic NOR gate

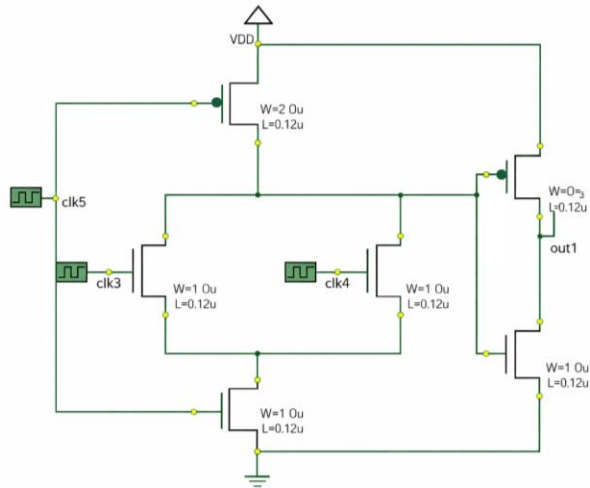
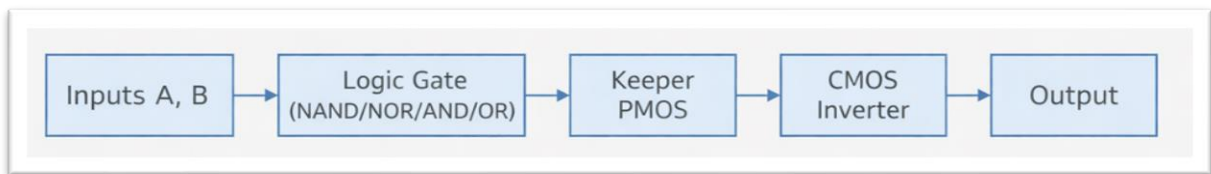


Figure 5. Dynamic logic OR gate

Block Diagram :



Expected Output :

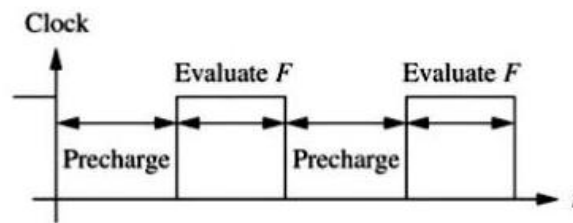
During the precharge phase (CLK = 0), the dynamic node is charged to the supply voltage (VDD), resulting in a HIGH output after inversion. During the evaluation phase (CLK = 1), the NMOS evaluation network conditionally discharges the dynamic node depending on the applied inputs.

The operation of each circuit will be verified by applying different input combinations and observing the corresponding outputs. The output levels remain clearly distinguishable, with HIGH \approx VDD and LOW \approx 0V, and transitions synchronized with the clock, reflecting the precharge and evaluation phases.

Each logic gate will display distinct behaviour based on its configuration.

- NAND gate will produce a LOW output only when all inputs are HIGH.

- NOR gate will produce a LOW output when any one of the inputs is HIGH.
- AND and OR gates will be realized through domino logic structures followed by inverter stages.



Research Paper/Journal/etc. :

Title : Design and Implementation of Domino Logic Circuit in CMOS

Author : Ankita Sharma , Divyanshu Rao , Ravi Mohan

Link : <https://www.jncet.org/Manuscripts/Volume-6/Issue-12/Vol-6-issue-12-M-04.pdf>

Sources/References :

- <https://siliconvlsi.com/dynamic-cmos-logic/>
- <https://siliconvlsi.com/domino-cmos-logic/>
- <https://www.geeksforgeeks.org/electronics-engineering/difference-between-static-cmos-and-dynamic-cmos/>