Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant :

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Title of the circuit :

Design and Simulation of a Time-Frame Integrate-and-Fire (TIF) Neuron Circuit Using eSim

Theory/Description :

The Time-Frame Integrate-and-Fire (TIF) neuron circuit is a mixed-signal CMOS implementation of a spiking neuron model designed for hardware realization of spiking neural networks (SNNs). Unlike conventional integrate-and-fire neurons, the TIF neuron integrates synaptic input currents over a defined time-frame and generates output spikes in the subsequent time-frame, enabling synchronized and pipelined operation.

The circuit consists of an input integrator, charge-sharing mechanism, discharger, comparator, and spike generator. The input current is integrated onto a membrane capacitor (C1), after which the stored charge is transferred to a secondary capacitor (C2) through a charge-sharing process. A MOSFET-based discharger provides a controlled discharge current, creating a linear decay of the membrane potential. A comparator detects when the voltage exceeds a threshold and triggers spike generation.

This architecture improves energy efficiency and enables better compatibility with artificial neural network (ANN) operations such as bias addition and pooling. In this project, a simplified version of the TIF neuron circuit will be implemented using eSim, and transient simulations will be performed to analyze membrane voltage evolution, spike generation, and the relationship between input current and firing rate.

Reason to reproduce with eSim :

The TIF neuron circuit is well-suited for migration to eSim because it is composed of fundamental CMOS building blocks such as current mirrors, capacitors, MOSFET switches,

comparators, and logic gates, all of which can be implemented using open-source SPICE models.

Reproducing this circuit in eSim aligns with the objectives of the FOSSEE Research Migration Project by enabling open-source validation of a recent IEEE-published neuromorphic circuit. It also provides an accessible platform for students and researchers to study advanced analog and mixed-signal circuit design without relying on proprietary tools such as Cadence or Silvaco.

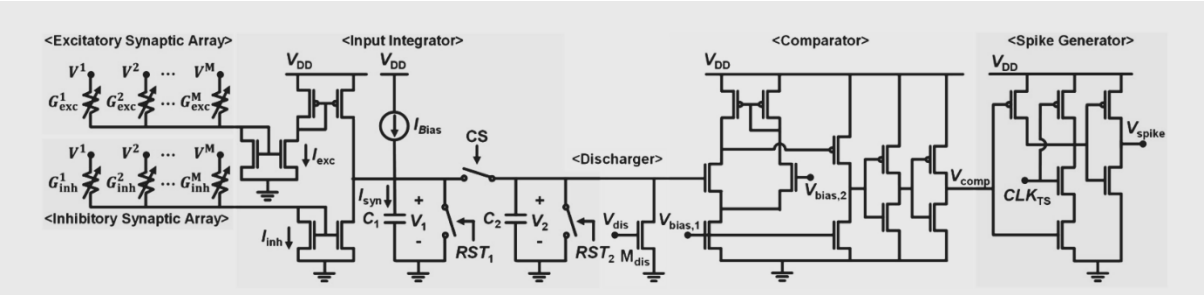
Expected Outcome/outputs :

The migrated circuit is expected to demonstrate correct transient behavior of a Time-Frame Integrate-and-Fire (TIF) neuron. Transient simulations will be performed to observe:

- Membrane voltage evolution across the capacitor during integration
- Threshold crossing and corresponding switching of the comparator
- Reset and discharge behavior of the membrane node
- Generation of output spike pulses in response to input current

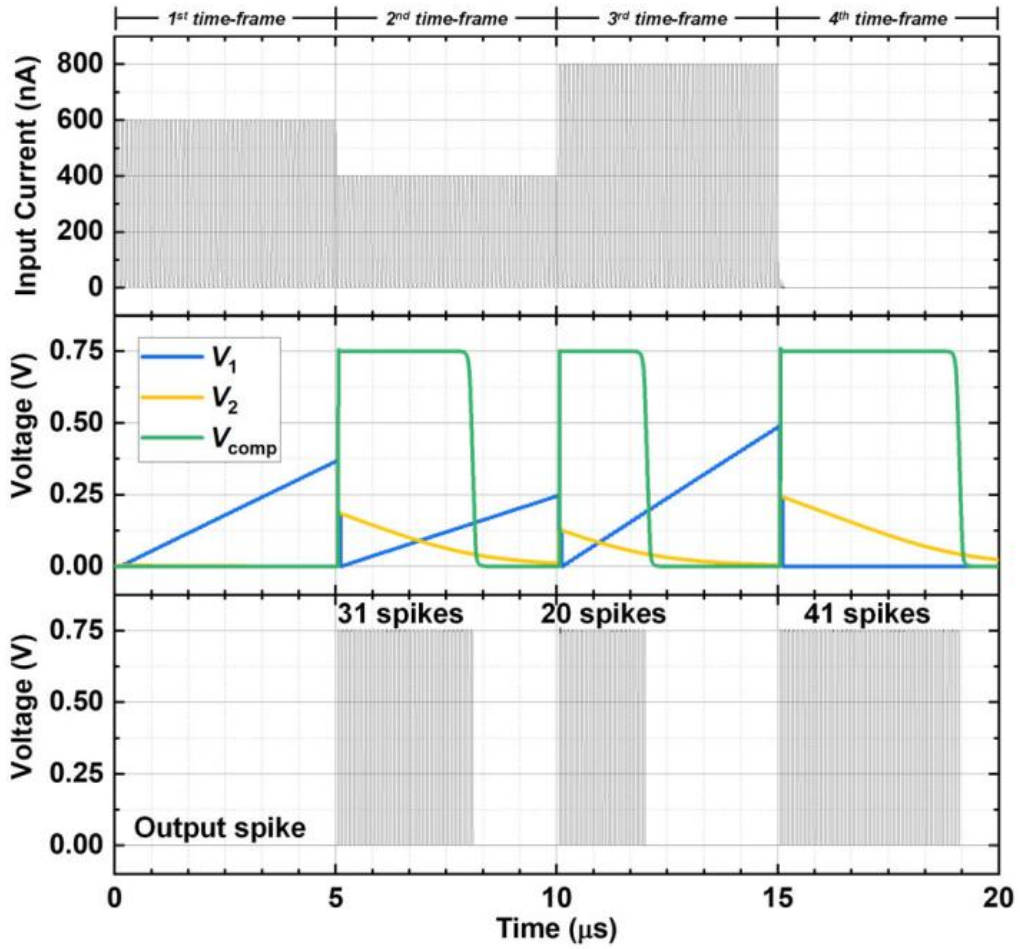
These results will validate the integrate-and-fire operation of the neuron circuit and confirm its functionality through time-domain waveform analysis.

Circuit Diagram(s) :



*refer the research paper 1 , figure 2.

Expected Results (Input, Output waveforms and/or Multimeter readings) :



*refer from the research paper(1), figure 5.

Research Paper/Journal/etc. :

1) Yeonwoo Kim, Bosung Jeon, Jonghyuk Park, and Woo Young Choi, "Time-Frame Integrate-and-Fire Neuron Circuit for Low Energy Inference Hardware Spiking Neural Networks," *IEEE Access*, vol. 13, 2025. DOI: 10.1109/ACCESS.2025.3548318

2) Source/Reference(s) :

1) Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGraw-Hill, 2nd Edition.

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.