SIMULATION OF LOW AREA AND HIGH SPEED NINE PORT NETWORK-ON-CHIP ROUTER ARCHITECTURE

Pruthvija B
Dept, of TCE, (VTU)
RVCE (VTU)
Bengaluru, India
pruthvija 94@gmail.com

Ojashwini R N
Dept.of TCE,(VTU)
RVCE,(VTU)
Bengaluru, India
ojashwini21@gmail.com

G Ranjani
Dept. of TCE,(VTU)
RVCE,(VTU)
Bengaluru, India
ranjanig.rvce@edu.in

Abstract— **In present technological world, life demands very high speed gadgets which are requisite components of modern human existence to reduce accomplishment of habitual works. Accordingly, such devices should be capable for operating at expeditious. Conventionally multi-core processing architecture is been used to increase this operational speed. In such instant, the total task should be divided into sub-smaller tasks and those particular smaller tasks has to be executed parallel by each processing cores respectively. In order to calculate approximate value of complete performed tasks has to be shared among individual processor. There-upon, bi-directional communication is peremptory between all these processing elements, which are been present in multi-core system. Normal bus architecture could not support this class of communication resulting many issues, hence Network-On-Chip (NoC) router acceptable. In these present work, 3X3 router arrangement considering mesh topology which is area efficient router architecture for NoC is designed using FPGA.**

Keywords—Network on chip, Routing, System on chip, Intellectual Property, FIFO, topology, Channel selection, Routers.

I Introduction

Network-On-Chip is a conveyance subsystem on an integrated chip in between the Intellectual Property (IP) propound in a System-On-chip[1 and 10]. System comprises of many IP blocks on a SoC. Hence data fetching from one IP blocks to another IP blocks increases exponentially. Present bus architecture may not able to sustain this large amount of data transfer without reducing device operating frequency. Hence NoC is slowly being gain and foremost paradigm for executing communication among IP cores in SoC. While complexity of system increases exponentially with wired connection throughout core. Consequently, resolute wires possess reusability and workability. An allocated bus is position which is habitual to miscellaneous cores. The resemble of allocated bus is more workable and is thoroughly reusable, but allows only one conveyance transaction at a time, each core allocate the similar relay bandwidth in system and its extensible is restricted to less dozen IP cores. Thus, ascendable was major issue with buses.

NoC architecture is been an elevated performance, ascendable and power efficient substitute for SoC, which provides solutions by reinforcing multiple contemporaneous connections with different systems. The system which are unified with NoC is been easily substituted with other IP cores systems of any vendor that are available in market.

Hence this NoC is ideally convenient for integrated systems which can separates computation part and communication part for complexity of systems. So NoC concern with utmost case without any interference in computation part. Furthermore, efficient routing algorithm add-up to increase in efficiency of network embedded on chip. In following proposed router architecture mesh topology in consideration with XY routing algorithm to satisfy performance requirement that implements NoC such as low latency, guaranteed throughput, sufficient transfer capacity for faster transferring of data via specified path between source and destination by selecting shortest path in network and scheduler to avoid collision and delay is presented. In fig 1, shows conceptual view of nine port Network on Chip router which comprises of main building blocks namely links, routers and network adapter.

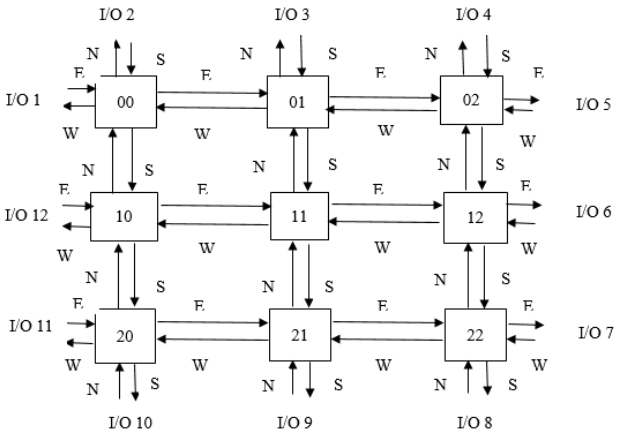


Fig 1: Nine port Network on Chip Router

II Literature Survey

A new pipelined router designed in [1], focused on minimizing latency of router. Critical paths are considered by router frequency bounded to those router components. Primarily adding onto the limitation is performance of router called

978-1-5386-2440-1/18/$31.00 ©2018 IEEE

arbiter, hence multiple smaller arbiters was designed. Solution for fault-finding communication problem between multiple IP cores was given [2]. In [3], a reconfigurable router architecture which is modified NoC for SoC design, where each buffer depth used in input channels can be reconfigured along with handshaking mechanism. In [4] postulates a layered design of re-configurable micro-networks, which exploits methods and tools for general networks. Paper [5] presented adaptive routing algorithm for fault tolerance which do not require virtual channels. Method to increase throughput has been presented in [6] which provide tools for automation execution for complete synthesis flow. In order to optimize the path selection complexity level, a master and slave router condition for single router data process was implemented in [6]. A generic network interface and router architecture involving fundamental NoC techniques by adopting clock and low power efficient techniques were implemented in [7].

The main objectives of this project are to study the NoC components, parameters and applications, study the Router architecture for NoC, to design a Dynamic FIFO using VHDL and to analyze the obtained simulation results.

III Proposed Architecture

The proposed NoC router architecture block diagram is as shown in fig 2, consisting of four FIFO and controller unit. The propound block have both input and output ports in all four directions namely East, West, North and South. Control logic is designed such that one of the four-input data is inserted in small amount by FIFO. FIFO in this work is designed to detect whether respective port is full or empty depending on the data arrival to certain block (router). These blocks are mainly designed to avoid collision data which is major concern in communication networks.

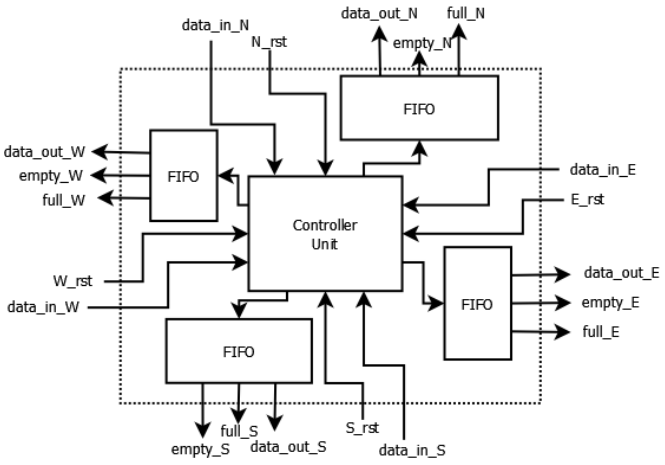


Fig 2: Proposed Block Diagram

The block diagram shows the nine port NoC router arranged as above, which is placed as node position such as 00, 01, 02, 10, 11, 12, 20, 21, and 22. Each router will consist of 4 channels namely North, East, West and South. Each router consists of one input and one output port excluding corner router. The input to certain router will consists 13 bits which of enable input, destination ports (i.e., dx and dy) and 8 bits data. The data format is as shown in fig 3

Enable	dx	Data	Dy
(1 bit)	(2 bits)	(8 bits)	(2 bits)

Fig 3: Data format

The corresponding router which is selected as source point should be enabled by setting enable bit of certain router as '1' and all other router's enable bit as '0'. Following with enable bit, the destination address is identified by router. The router consists of following blocks

1. Routing Block
2. Channel Selection block
3. Controller Unit.
4. FIFO

Routing Block

In Network on Chip, routing must be done for connecting distinctive components all together in most efficient way. For this instance, choosing shortest path adequacy be insistent in one circumstanstances, although fabricating a proper activity amount of adjusting might be of most prominent intendment in other outlook. An immense routing algorithm is being admitted and each one possesses few advantage and disadvantages in contrast. The routing block of NoC is as shown in fig 4.

The XY routing algorithm is one among distributed deterministic algorithm. Live-lock and dead-lock do not occur at no time in XY routing algorithm. This routing algorithm [8] is best suited for Network on Chip implemented by using mesh topology. The data packet present at node or router are firstly routed towards X direction and then Y direction. Horizontal movement of data packets are represented by X direction and Y direction movement of data packets are represented by Y direction towards destination router. Since router address are placed in XY co-ordinates.

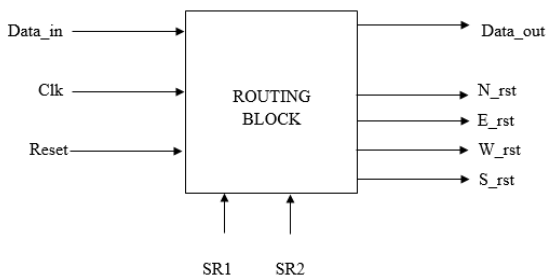


Fig 4: The routing block of NoC

The Network on Chip consists of nine routers where on router consists of four FIFO blocks.

Each router possesses 4 directions namely East, West, North and South. The 13 bit of data is transmitted from chosen router called source router. This routing block consists of 4 inputs which are Data_in, clock, reset and source address. The outputs of routing block are Data_out and reset outputs of all for channel i.e., N_rst, E_rst, W_rst, S_rst.

Suppose destination address is 12, then coding is done in such a way that each bit is coded in binary format where

$$1 \rightarrow 01 \text{ and } 2 \rightarrow 10$$

Hence dx = 01 and dy = 10.

Initially this block checks for reset pin and then enable pin. The routing block transmits data only if reset pin is '0', and enable pin is '1'. If not complete NoC is reset to '0'. This blocks divides given data format into enable bit, destination bits and data bits. This block also consists of source address namely sr1 and sr2 which is been coded already depending on source position of selected router which is same as destination point selection.

Algorithm

1. Suppose 'dx' is greater than 'sr1', then data is transmitted towards south direction.
2. If 'dx' is lesser than 'sr1', then North Channel is selected.
3. In case 'dx' = 'sr1' then, compares 'dy' with 'sr2'
4. If 'dy' is greater than 'sr2', then data is transmitted towards east direction.
5. Else west channel is activated.

Controller Unit

Controller unit mainly consists of following blocks namely D Flip flops, multiplexers, de-multiplexers and demux-controller as shown in fig 5. This designed controller unit concerned on controlling the data flow direction across router by monitoring all ports for representing data flow in individual directions. To synchronize all intermediate data with clock signal D Flip-flops is used. Enabling of D Flip-flop is monitored by De-mux which is in-turn controlled by De-mux controller in accordingly towards destination address which simultaneously activates D Flip-flop direction in transmit the data in specified direction.

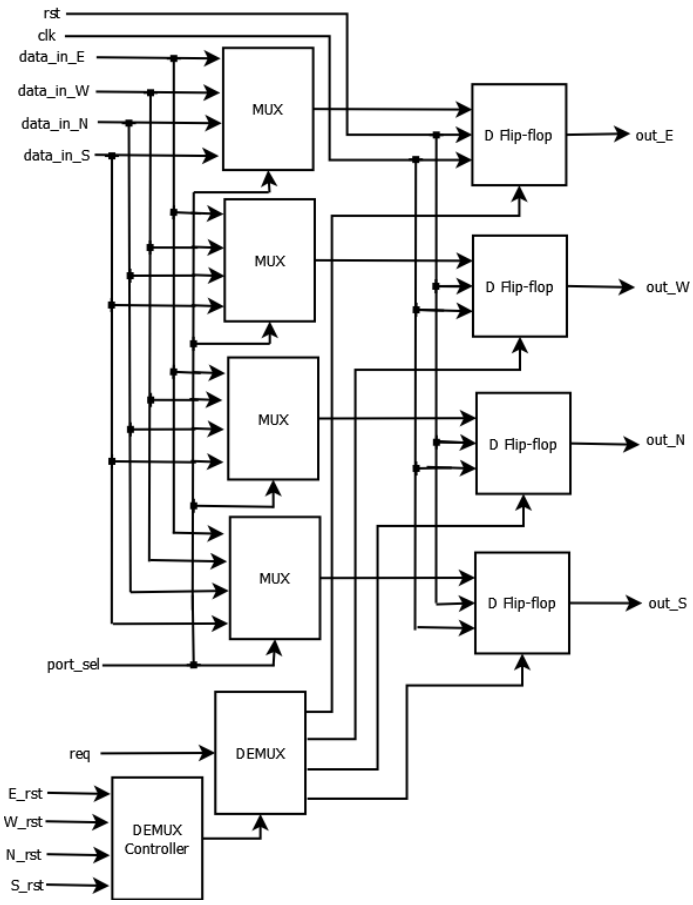


Fig 5: Internal Structure of Proposed Controller Unit

FIFO

FIFO designing block diagram is as shown in fig 6. Main purpose of FIFO is to be temporarily hold the data packets for pre-requisite period and routing to corresponding nest destination.

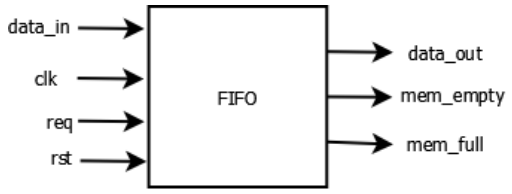


Fig 6: Block Diagram of FIFO

The internal edifice of designed FIFO is as shown in fig 7, which primarily consists of 3 D flip-flop which are mainly memory building blocks which also called as FIFO depth [9]. The corresponding decision and counter block are used to signify memory status (i.e., full or empty) for each FIFO block.

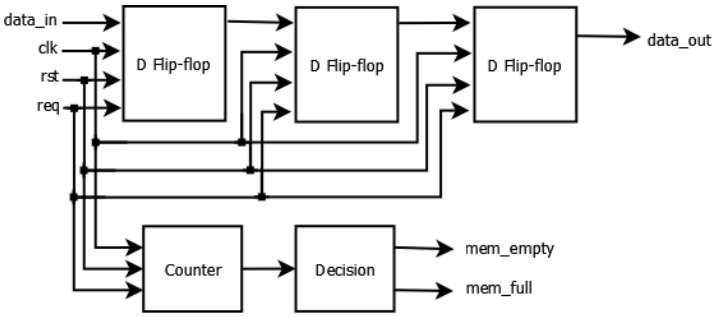


Fig 7: Internal Structure of FIFO

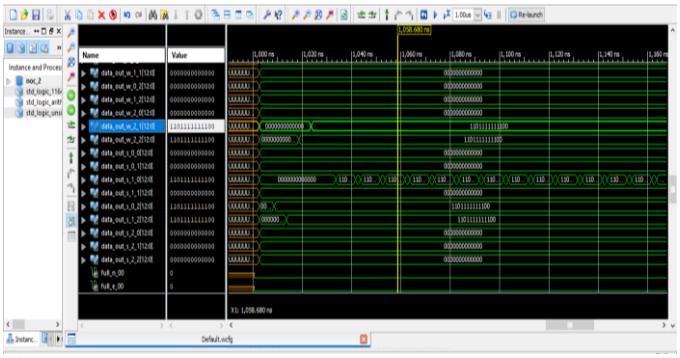


Fig 8: Simulation results of obtained output

IV Results

The proposed architecture is simulated using Xilinx 14.5 software and simulation is checked by ISim simulator P.58f version. The coding of the architecture is done using VHDL language.

Assuming the data transmitted by input 4 (i.e., n_0_2) i.e., to router 02 towards router 22 as shown in fig 7, the data travels in shortest path considering the OS scheduling at corresponding instants designed by XY routing algorithm and reaches the specified destination port.

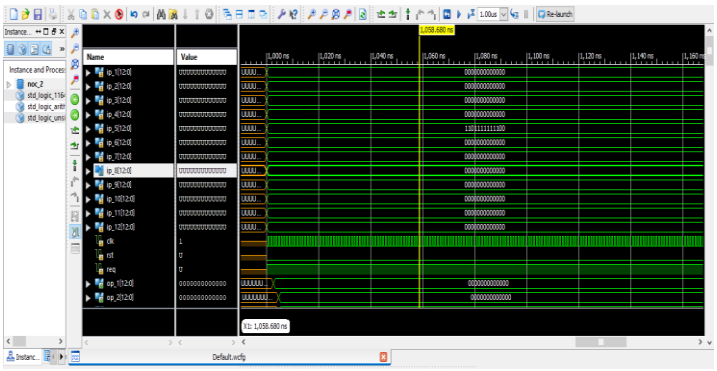
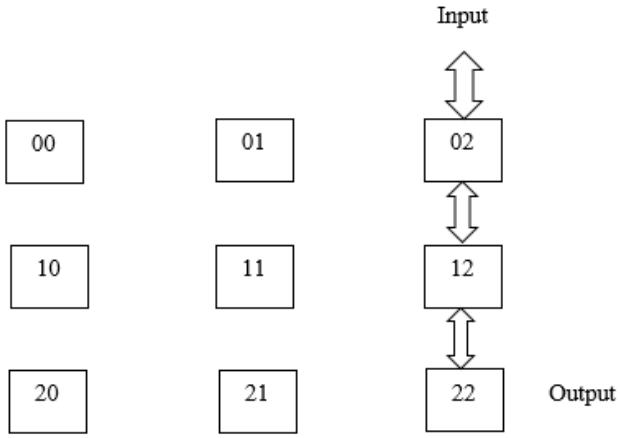


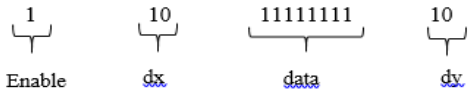
Fig 7: Input Waveform

The data travels over several nodes to reach destination port. This algorithm provides two-way communication, where same data is transmitted and received is each node at the data transmitted. By checking whether the FIFO is full or empty, the data is stored in it. Finally, the data is transmitted to given destination port as shown. Here the one router uses adjacent router FIFO to reduce deadlock which results in the data loss as shown in fig 8. The bi-directional data transfer is because during data packets movement the sent node should be acknowledge.

Note down the internal ports outputs and draw the shortest path selected by data packets for its transmission.



- Initially input is loaded to ip_4 which is to router 02 from north direction as



- If enable is '1' then certain router is active, and router 02 is initialized.
- For ip_4, SR1=00 and SR2 = 10
- Compare dx and SR1

  dx > SR1, hence south channel is triggered using channel selection block.

- The data packets of 13 bits is transmitted to router 12, now router 12 becomes source router and router 22 will be the destination router.

The data packets travel through several as explained before and finally reaches destination node with all data of 13 bits.

Synthesis Report

The propound NoC architecture uses 2016 slice registers, 984 slice LUT's and 735 LUT-FF pairs. The maximum operating frequency is 244.248 MHz.

Table 1: Device utilization summary of Proposed architecture

Parameters	Device Utilizations
Number of slice registers	2016
Number of Slice LUT's	984
Number of full used LUT-FF pairs	735
Maximum Operating Frequency (MHz)	244.248

V Conclusion

In this paper, nine port Network on chip router is proposed which been able to transfer data in bi-directional manner operating at high speed consuming less area since it consists of logical elements occupying less space on chip and works at a high speed. This proposed model can be implemented for 4X4 routing with slight modification during coding. The deadlock and livelock problem which are familiar during routing of data packets is almost eliminated. Since the architecture uses digital logic elements like D Flip-flop, demultiplexers, multiplexers which is also suitable for VLSI implementation.

VI Acknowledgment

The author would like to thank Guides for helpful discussion.

References

[1] M. Dehyadgari, M. Nickray, A. Afzali-kusha, Z. Navabi: "Evaluation of Pseudo Adaptive XY Routing Using an Object Oriented Model for NOC". *The 17th International Conference on Microelectronics*, 13–15 December 2015.

[2] H. Kariniemi, J. Nurmi: "Arbitration and Routing Schemes for On-chip Packet Networks. Interconnect-Centric Design for Advanced SoC and NoC" (toim: J. Nurmi, H. Tenhunen, J. Isoaho & A. Jantsch), *Kluwer Academic Publishers*, 2014, pages: 253–282.

[3] R. Kumar, V. Zyuban, and D. M. Tullsen. "Interconnections in multi-core architectures: Understanding mechanisms, overheads and scaling". *Proceedings of the 32nd Annual International Symposium on Computer Architecture*. 2015.

[4] V. Soteriou, H. Wang, L. S. Peh. A statistical traffic model for on-chip interconnection networks. *Proceedings of the 14th IEEE International Symposium on Modeling*, "Analysis, and Simulation of Computer and Telecommunication Systems" (MASCOTS'06). Sept. 2016, pp. 104-116.

[5] D. Seo, A. Ali, W.-T. Lim, N. Rafique. "Near-optimal worst-case throughput routing for two-dimensional mesh networks". *Proceedings of 32nd International Symposium on Computer Architecture, 2005*. ISCA '05. pp. 432 - 443.

[6] E. Nilsson, M. Millberg, J. Öberg, A. Jantsch. "Load distribution with the proximity congestion awareness in a network on chip". *Proceedings of the Desin Automation and Test in Europe Conference and Exhibition*. 2013, pp. 1126-1127.

[7] Liang, J.; Swaminathan, S.; Tessier, R. "aSOC: A Scalable, Single-Chip communications Architecture*". In: IEEE International Conference on Parallel Architectures and Compilation Techniques*, Oct. 2010, pp. 37-46.

[8] Ni, L. M.; McKinley, P. K. "A Survey of Wormhole Routing Techniques in Direct Networks*". IEEE Computer Magazine*, v.26(2), February, 2013, pp. 62-76.

[9] Mohapatra, P. "Wormhole routing techniques for directly connected multicomputer systems". *ACM Computing Surveys*, 30(3), Sep. 2011, pp 374-410.

[10] Bolotin, E.; Cidon, I; Ginosar, R.; Kolodny, "A. QNoC: QoS architecture and design process for Network on Chip". *The Journal of Systems Architecture, Special Issue on Networks on Chip*, 2014.