Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant: **Samiksha Biswas**

Affiliation / Institution: **Department of Electrical, IIT(ISM) Dhanbad, Dhanbad, Jharkhand, India**

Title of the circuit: Soft-Switching SiC Interleaved Boost Converter

Theory/Description:

The circuit is a soft-switching Silicon Carbide (SiC) interleaved boost converter that integrates the theoretical advantages of the Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ) topology with a dual interleaved boost converter using an interphase transformer (IPT). This configuration is designed to increase power density and operating frequency by significantly reducing switching losses and limiting the high dv/dt typically associated with SiC devices

Key Components:

- Main Switches (Q_1–Q_4): High-power SiC MOSFET modules utilized in a bidirectional or step-up configuration.
- Auxiliary Circuit: Comprises a single auxiliary inductor (L_1), auxiliary switches (Q_{1A}, Q_{2A}), and diodes (D_{AUX1}, D_{AUX2}).
- Snubber Capacitors (C_{S1}, C_{S2}): Connected in parallel with main switches to facilitate soft switching; these are often formed entirely by the inherent output capacitance of the SiC MOSFETs.
- Interphase Transformer (IPT): Used to balance currents between the interleaved legs and double the effective ripple frequency

Operation:

The circuit operates as a soft-switching SiC interleaved boost converter by integrating the Snubber Assisted Zero Voltage and Zero Current Transition (SAZZ) topology with a dual interleaved boost structure utilizing an interphase transformer (IPT). To facilitate Zero Voltage and Zero Current Transition (ZVZCS), an auxiliary switch is activated shortly before the main switch to initiate a resonant discharge process. During the initial sub-period, the auxiliary inductor (L_1) restricts the rate of current change, ensuring the auxiliary device turns on with Zero Current Switching (ZCS). This is followed by a resonant phase where the

snubber capacitor (which can be the inherent output capacitance of the SiC MOSFET) discharges through the auxiliary circuit until the voltage across the main switch drops to zero. Consequently, the main switch can be turned on under Zero Voltage Switching (ZVS) conditions, effectively eliminating turn-on losses. At turn-off, the snubber capacitors provide soft-switching conditions for the main devices, and the energy previously stored in the device output capacitance is recovered during the next turn-on cycle rather than being dissipated as heat. This interleaved operation balances currents through the IPT while halving the dv/dt compared to hard-switched alternatives and significantly enhancing overall efficiency.

Reason to reproduce with eSim :

Replicating the soft-switching SiC interleaved boost converter in eSim provides an additional layer of independent validation beyond the original LTspice results. While the initial study shows strong agreement between LTspice simulations and experimental data, implementation in the Ngspice-based eSim environment enables cross-platform verification of the design.

Consistent results across both simulation frameworks confirm that key performance characteristics—such as Zero-Voltage Zero-Current Switching (ZVZCS), reduced switching losses, and efficiency approaching 98%—are intrinsic to the converter topology rather than dependent on a specific SPICE engine.

Furthermore, eSim's open-source architecture improves transparency in numerical methods, device modelling, and convergence behaviour. This enhances reproducibility and allows deeper inspection of simulation fidelity compared to proprietary tools.

Successful validation of transient phenomena, including resonant transitions, dv/dt reduction, and energy recovery, within eSim reinforces the robustness of the design. It demonstrates that the converter's performance is fundamentally tool-independent, supporting its applicability in future research and high-efficiency power electronics development.

Expected Outcome/Outputs:

The implementation is considered successful if it meets the following performance metrics:

- Total Loss Reduction: The converter should reduce total losses from approximately 293.5 W (hard-switched) to 224 W (soft-switched).
- Efficiency: The experimental efficiency is expected to be approximately 98% at rated power, with simulation efficiency reaching up to 98.7%.
- Thermal and Reliability Improvements: By eliminating turn-on losses and reducing turn-on dv/dt by 50%, the circuit demonstrates improved reliability for inverter-fed electrical machines and reduced EMI generation compared to standard SiC boost converters
- Switching Timing Verification: The implementation validates the required advance delay between auxiliary and main switch turn-on (≈0.4–0.45 μs), ensuring proper sequencing for achieving ZVZCS operation as demonstrated in the paper

Circuit Diagram:

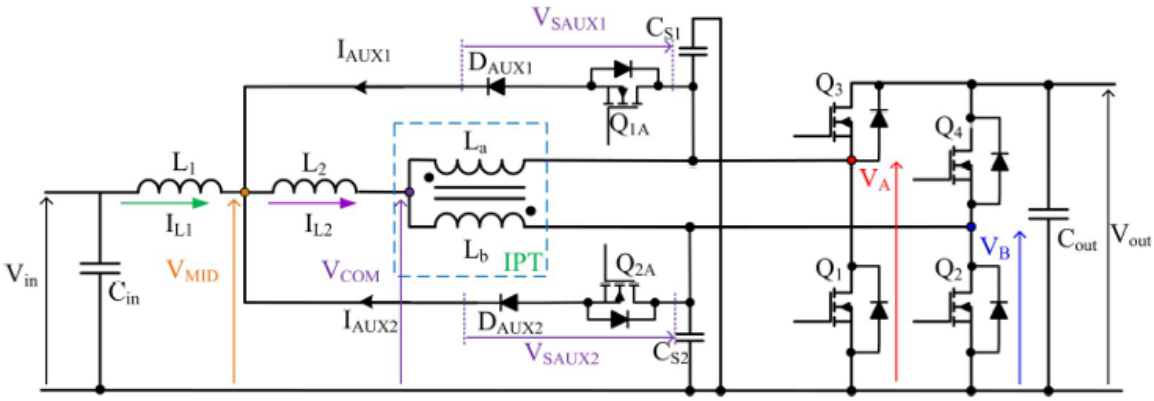


Fig. 1. Circuit schematic.

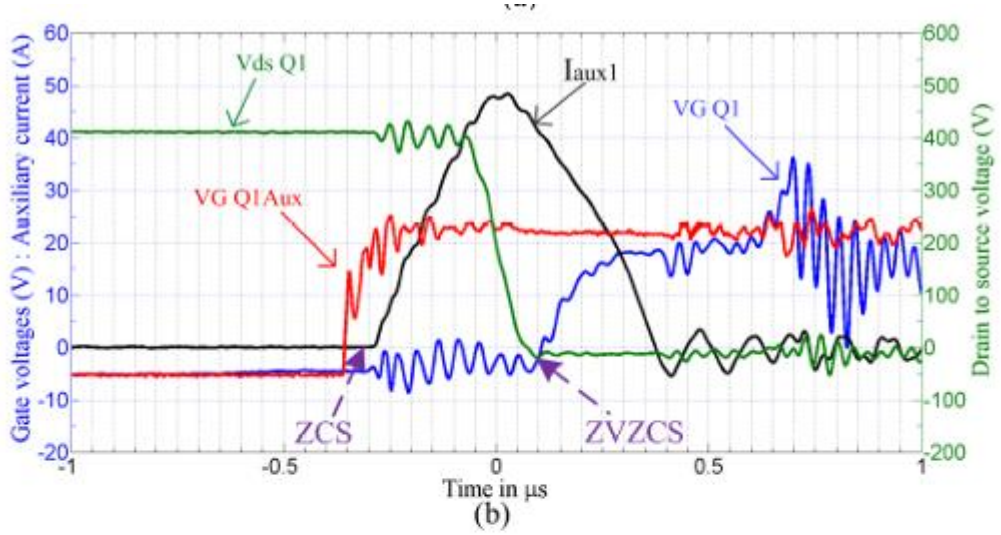
Expected Results (Input, Output waveforms and/or Multimeter readings):

Operating Parameters and Levels:

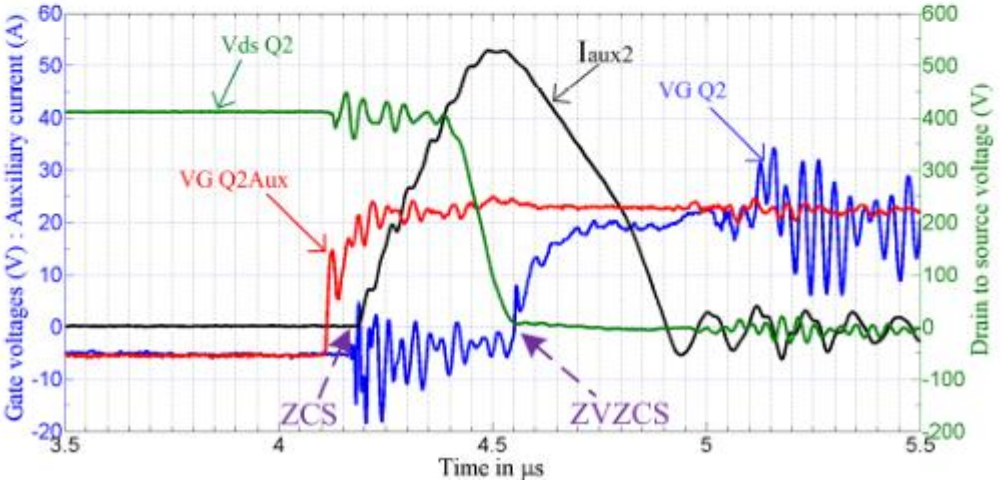
1. Input Voltage (V_{in}): Approximately 174 V (tested range 100 V to 174 V)
2. Output Voltage (V_{out}): Stepped up to 400 V–410 V.
3. Power Level: Rated at 12.5 kW to 12.9 kW.
4. Switching Frequency: Operating at 112 kHz.
5. Current Levels: Average Input Current ($I_{in(avg)}$) ~72.3 A to 74.1 A.
6. Output Current (I_o): ~30.8 A to 31 A.

Expected Waveform Shapes:

1. Gate Signals: The auxiliary switches (Q_{1A}, Q_{2A}) should show a pulse 0.4 µs to 0.45 µs (advance time) before the main switches (Q_1, Q_2) to initiate the soft-switching resonant process.
2. Main Switch Voltages (V_A, V_B): These should exhibit a trapezoidal shape, transitioning between 0 V and V_{out}. Notably, the turn-on dv/dt should be approximately 3.3 kV/µs, which is half the rate of a hard-switched converter (6.6 kV/µs).
3. Inductor Currents (I_{L1}, I_{L2}): These will display a triangular ripple. Due to the interleaving and the interphase transformer, the effective input and output ripple frequency will be twice the switching frequency (224 kHz).
4. Auxiliary Currents (I_{AUX1}, I_{AUX2}): These appear as resonant half-sine pulses during the turn-on transition. They should rise from zero (Zero Current Switching) and fall back to zero before the main conduction period ends.
5. Resonant Discharge: The voltage across the main switches (V_{ds}) must drop to 0 V before the gate signal (V_g) is applied, confirming Zero Voltage Switching (ZVS).



(b)



Research Paper/Journal/etc. :

Title : Soft-Switching SiC Interleaved Boost Converter
Author : M. R. Ahmed, G. Calderon-Lopez, F. Bryan, R. Todd and A. J. Forsyth
Page No. : 1 to 7
Link : (Direct link to IEEE)