Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : Nabajyoti Gogoi

Affiliation / Institution : Department of Electronics and Communication Engineering, NIT Silchar, Silchar, Assam, India

Title of the circuit : Design and Implementation of a T Flip-Flop Using JK Flip-Flop

Theory/Description : A flip-flop is a bistable sequential circuit used to store one bit of binary information. Among various types, the T (toggle) flip-flop is widely used in counters and sequential logic systems due to its ability to change state on every clock pulse when enabled.

In this project, a T flip-flop is implemented using a JK flip-flop by exploiting the characteristic behavior of the JK configuration. The JK flip-flop has two inputs, J and K, and its next state depends on the combination of these inputs and the current state.

To realize a T flip-flop using a JK flip-flop, both inputs are tied together and driven by the T input:

- **J = T**
- **K = T**

With this configuration:

- When **T = 0**, both J and K are 0, and the flip-flop maintains its current state (no change).
- When **T = 1**, both J and K are 1, causing the flip-flop to toggle its state on every active clock edge.

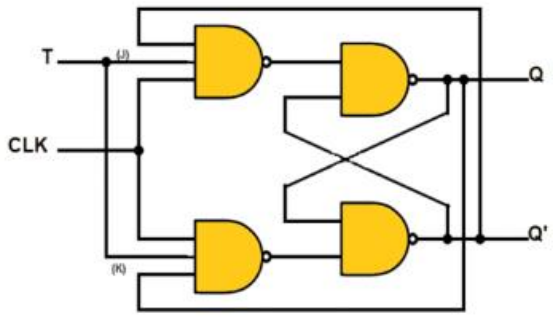
Thus, the JK flip-flop effectively behaves as a T flip-flop under this condition. The output toggles between logic high and low states in synchronization with the clock signal when enabled.

This implementation demonstrates how a more complex flip-flop (T) can be derived from a universal flip-flop (JK), highlighting the flexibility and importance of JK flip-flops in digital circuit design.

Reason to reproduce with eSim : This circuit is well-suited for implementation in eSim as it involves fundamental digital components and sequential logic design. Using eSim allows open-

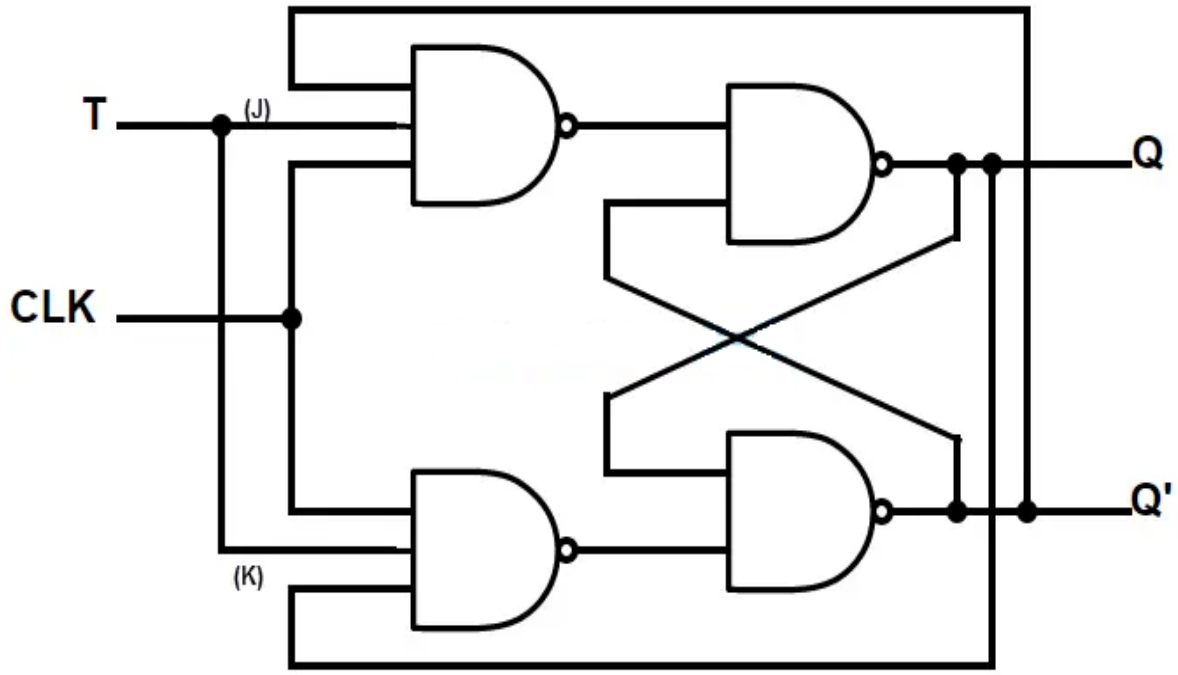
source simulation of flip-flop behavior without relying on proprietary tools. The project provides strong educational value by helping users understand flip-flop conversion techniques and timing behavior. Additionally, simulation in eSim enables easy verification of logic functionality and waveform analysis, making it ideal for academic and research purposes.

Expected Outcome/outputs : The implemented circuit is expected to behave as a T flip-flop. When the input T is low, the output will remain constant regardless of clock pulses. When T is high, the output will toggle with every active clock edge. The simulation will validate correct logical operation and demonstrate proper synchronization with the clock signal.



T	Q	Q'
0	0	0
1	0	1
0	1	0
1	1	0

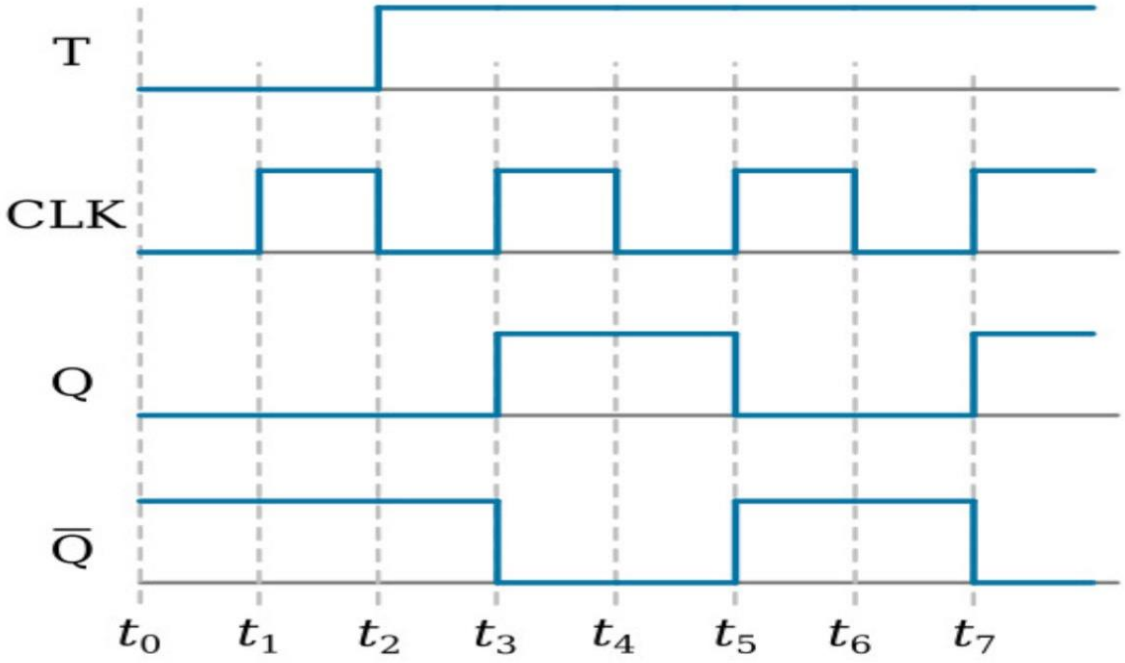
Circuit Diagram(s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :

- For T = 0: Output waveform remains constant (no change in Q)
- For T = 1: Output waveform toggles at every clock edge
- Clock signal: periodic square wave

• Output waveform: synchronized with clock transitions • Proper timing relationship between input, clock, and output will be observed



Research Paper/Journal/etc. :

Title : Designing an Efficient Approach for JK and T Flip-Flop with Power Dissipation Analysis Using QCA
Author : Shraddha Pandey, Sonali Singh and Subodh Wairya
Link:https://www.researchgate.net/publication/304991620_Designing_an_Efficient_Approach_for_JK_and_T_Flip-Flop_with_Power_Dissipation_Analysis_Using_QCA

Title : A Study of JK and T Flip-Flops with and without Delay Using QCA
Author : Aditi Bal, Subhashree Basu, Supriyo Sengupta
Link: https://www.iosrjournals.org/iosr-jvlsi/papers/vol4-issue6/Version-1/K04617076.pdf