Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Compact Discrete-Time Chaotic Oscillator Using 180nm CMOS Technology for True Random Number Generation

Theory/Description :
A True Random Number Generator (TRNG) is a hardware circuit that produces unpredictable binary sequences by harnessing physical randomness. Unlike Pseudo-Random Number Generators (PRNGs) that rely on deterministic algorithms, TRNGs harvest entropy from highly unpredictable physical phenomena, rendering them mathematically immune to predictive exploitation.

The proposed circuit implements a discrete-time chaotic oscillator based on a three-transistor CMOS nonlinear core, following the architecture of Priya et al. (2017). The circuit's nonlinear dynamics exhibit the key property required for sustained chaos generation: a high-gain folding mechanism that ensures extreme sensitivity to initial conditions and permanent aperiodicity.

Functional Blocks:

- **Chaotic Core (V-Shape Map):** Consists of M1 (PMOS, W/L=100μ/0.36μ), M2 (NMOS, W/L=120μ/0.36μ), and M3 (NMOS current bias, W/L=80μ/0.18μ). It utilizes a specific active-load and source-follower arrangement to create a transfer function where sweeping the input voltage causes the output to initially decrease and then sharply increase, forming a "V" shape. This provides the necessary topological "stretching and folding."
- **Sample & Hold (S/H) Transmission Gates:** Built from complementary PMOS and NMOS pairs driven by anti-phase clocks. They capture the continuous-time analog voltage generated by the core at precise discrete intervals and hold it steady for processing.
- **Holding Capacitors (C_1 and C_2):** 100fF passive elements that store the discrete sampled analog voltage during the "hold" phase.
- **Buffer Amplifier:** Acts as an impedance bridge to isolate the sensitive holding capacitors, while applying a slight 1.05x voltage boost to compensate for physical energy losses (charge injection, parasitic leakage) in the analog feedback loop. This prevents chaotic damping.

The supply voltage is 1.8V, the bias VB=0.80V, and the circuit uses TSMC 0.18μm CMOS process parameters (BSIM3v3 Level 49 models). A small noise perturbation (20mV at 127 MHz) on the bias voltage models real-world thermal jitter.

Table 1: Circuit Component Specifications: Proposed vs. Baseline

Component	**Type**	**Value in Our Circuit**	**Unit**	**Original Paper Value**
MP1	PMOS Transistor	W = 100, L = 0.36	μm	W=4, L=0.18 (All PMOS)
MN2	NMOS Transistor	W = 120, L = 0.36	μm	W=2, L=0.18 (All NMOS)
MN3	NMOS Transistor	W = 80, L = 0.18	μm	W=2, L=0.18 (All NMOS)
MP4, MP6	PMOS Transistors	W = 4, L = 0.18	μm	W=4, L=0.18
MN5, MN7	NMOS Transistors	W = 2, L = 0.18	μm	W=2, L=0.18
C1, C2	Capacitors	100	fF	Not explicitly specified
E1	VCVS (Buffer)	1.05	Gain	Ideal Buffer (unity gain)
VDD_src1	DC Voltage	1.8	V	1.6 V
VB_DC1	DC Voltage	0.8	V	1 V (transient behavior)
V_NOISE1	AC Voltage	Amp=0.02, Freq=127	V, MHz	Not explicitly specified

Reason to reproduce with eSim :
This circuit is highly suitable for eSim migration because the original paper was simulated using HSPICE, a proprietary tool. Migrating to eSim using Ngspice with TSMC 0.18μm BSIM3 models demonstrates open-source equivalence. The circuit is purely analog CMOS with no special IP blocks, making it straightforward to implement. Furthermore, chaotic oscillators and TRNGs are an active research area with high educational value, and no such high-frequency, discrete-time CMOS chaotic circuit currently exists in the eSim Research Migration database.

Expected Outcome/outputs :
The simulation is expected to prove the existence of sustained, high-entropy chaotic behavior within the 180nm CMOS constraints. Expected graphical outputs generated via Ngspice include:

- **Dense Chaotic Waveform:** A full 5-microsecond transient plot showing an extremely dense, aperiodic voltage variation between 0.4V and 1.6V, visually confirming high-entropy behavior without limit cycles.
- **Zoomed Chaotic Stepping Detail:** A 0.5-microsecond window revealing the individual 10ns discrete-time sample-and-hold plateau steps driven by the 100MHz clock.
- **Phase Space / Strange Attractor:** A phase portrait plotting the input vs. the delayed node, displaying a dense, multi-layered chaotic "web" serving as definitive mathematical proof of sustained deterministic chaos.

Circuit Diagram(s) :
The visual representation of the chaotic oscillator is broken down into modular components to highlight the custom parameterization over the baseline literature.

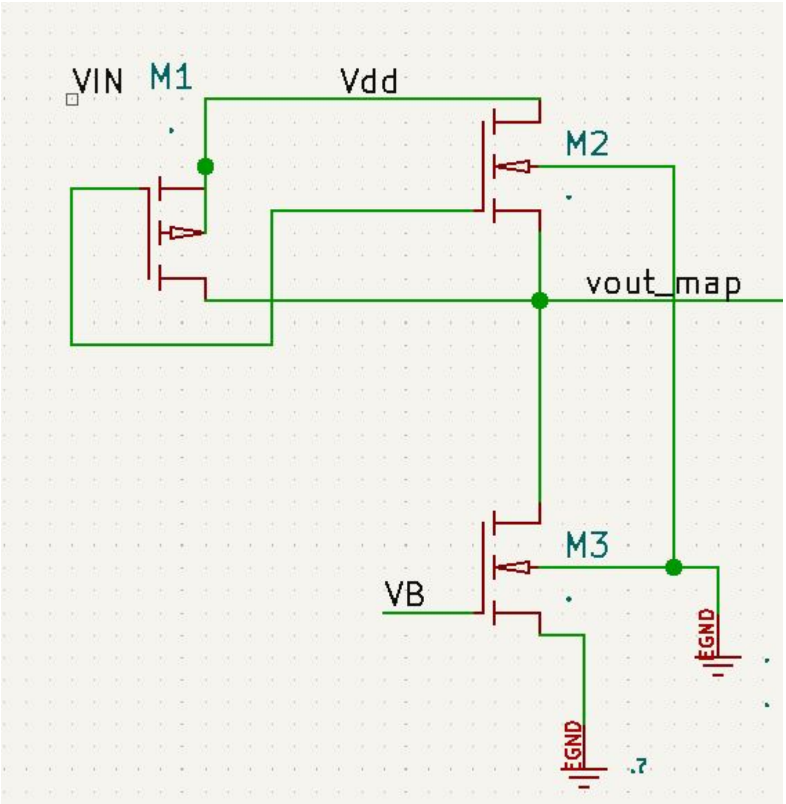


Figure 1: The redrawn isolated 3-transistor V-map core schematic. This non-linear mapping stage dictates the primary chaotic folding geometry. This is the exact circuit representation from the original paper.

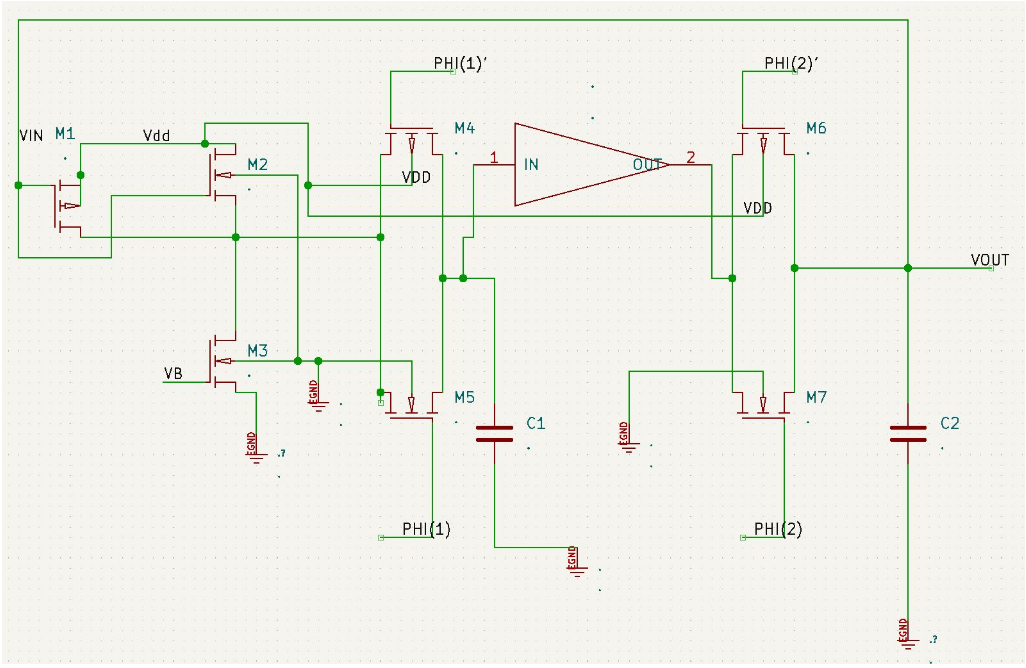
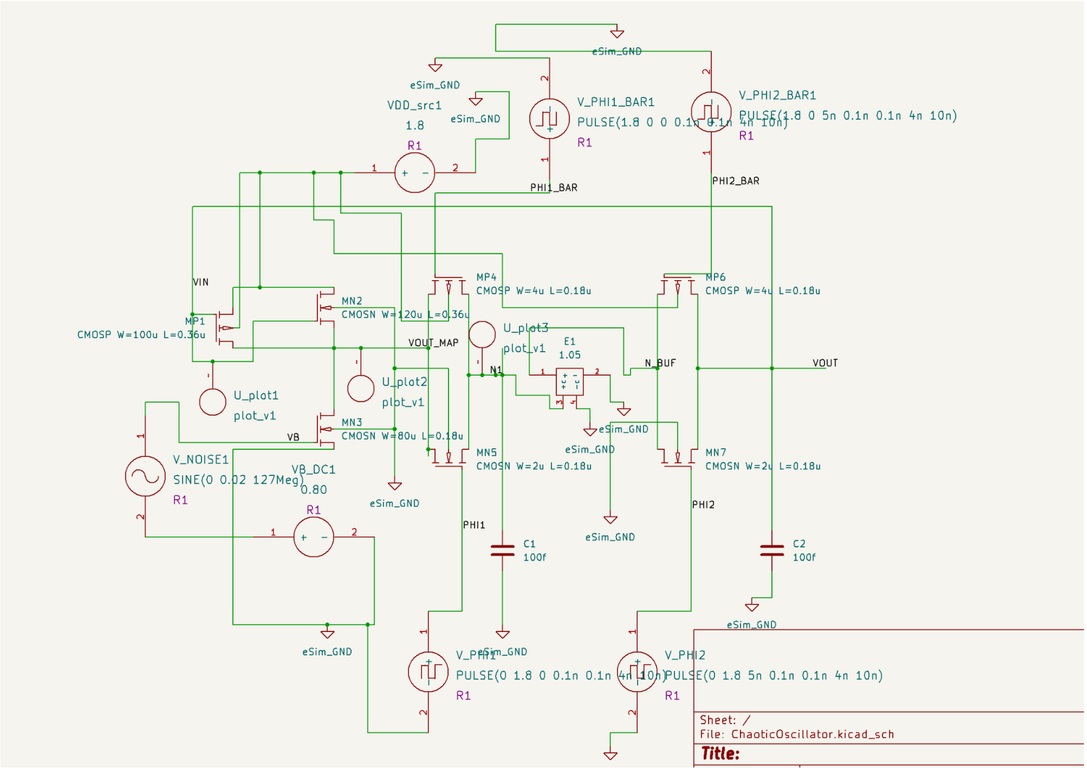
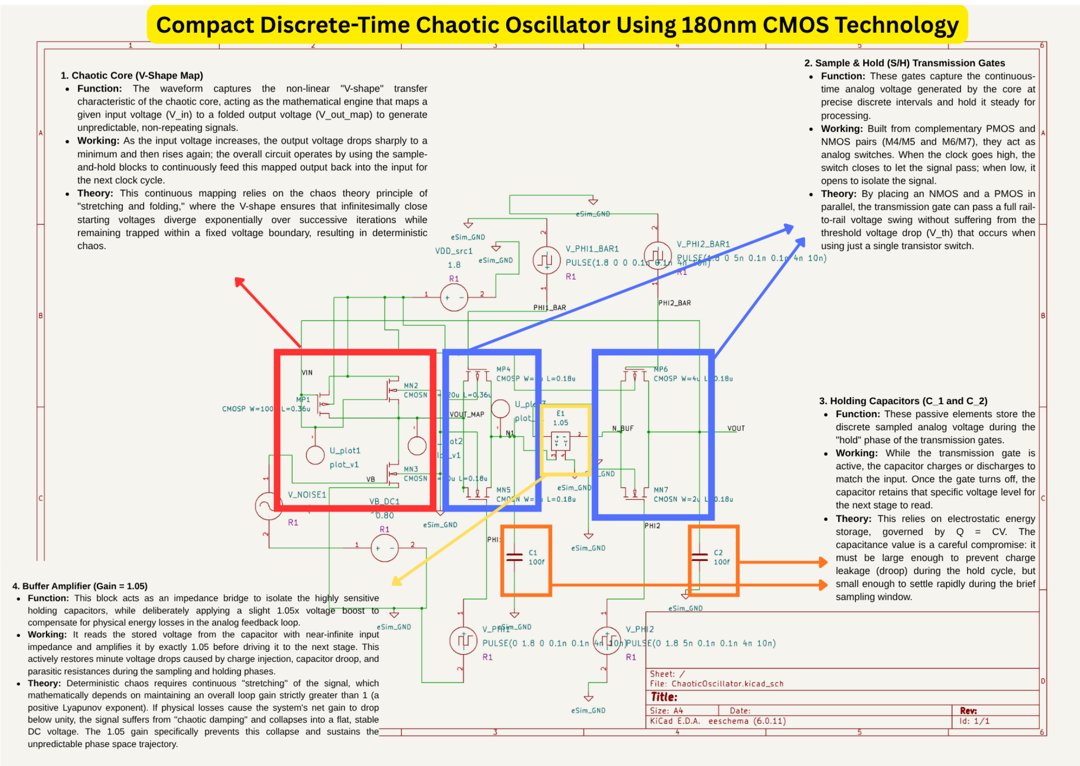


Figure 2: The complete, redrawn schematic of the discrete-time chaotic oscillator illustrating the integration of the V-map, two sample-and-hold transmission gate stages, and the 1.05x gain compensation buffer. This is the exact circuit representation from the original paper.



(a) Bare eSim schematic implementation.



(b) Annotated schematic highlighting individual functional blocks.

Figure 3: Our proposed equivalent circuit implemented for eSim. (a) The raw schematic capturing the custom parameterized design natively in KiCad. (b) The schematic partitioned to map the system architecture.

Block Diagram (s) :
The system architecture and signal flow of the discrete-time chaotic oscillator are visually mapped out below. The high-level block flow consists of: *Input (Feedback)* → *Three-Transistor Non-linear Map Core* → *S/H Transmission Gate 1* (ϕ_1) → *Holding Capacitor 1* → *1.05x Buffer* → *S/H Transmission Gate 2* (ϕ_2) → *Holding Capacitor 2* → *Output (Feedback to Input).*

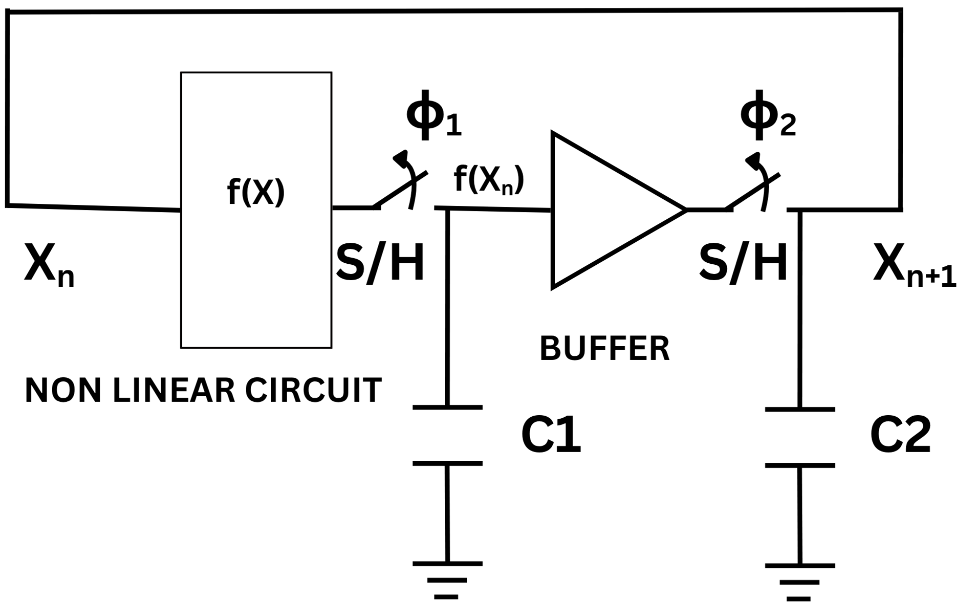


Figure 4: Redrawn High-level architectural block diagram of the discrete-time chaotic oscillator showing the non-linear circuit, sample-and-hold stages, buffer, and the global feedback loop.

Expected Results (Input, Output waveforms and/or Multimeter readings) :
Inputs: DC bias VB=0.80V with 20mV, 127MHz sinusoidal dither noise. VDD=1.8V. Two-phase non-overlapping clock at 100MHz (PHI1, PHI2 with complementary PHI1_BAR, PHI2_BAR). Initial condition applied via Ngspice: V(/VIN)=1.2V.
Outputs: A highly irregular, jagged voltage at the VIN node ranging approximately 0.4V to 1.6V. True chaotic behavior is confirmed by a complete lack of repeating periods in the time domain, cycle-to-cycle peak variance, and a dense strange attractor cloud in the VOUT_MAP vs VIN phase space.

Research Paper/Journal/etc. :
Title : Compact Chaotic Oscillator Using 180nm CMOS Technology for its Use in True Random Number Generator
Author : M. Priya, G. Swetha, R. Gupta, A. Pandey
Page No. : 366-370
Link : https://ieeexplore.ieee.org/document/8378183

Source/Reference(s) :

- P. Dudek and V. D. Juncu, "Compact discrete-time chaos generator circuit," *Electronics Letters*, vol. 39, pp. 1431-1432, 2003. DOI: 10.1049/el:20030881.