Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit: Research Migration of a High-Efficiency Leading-One Detector (LOD) Based shift-and-Add Multiplier

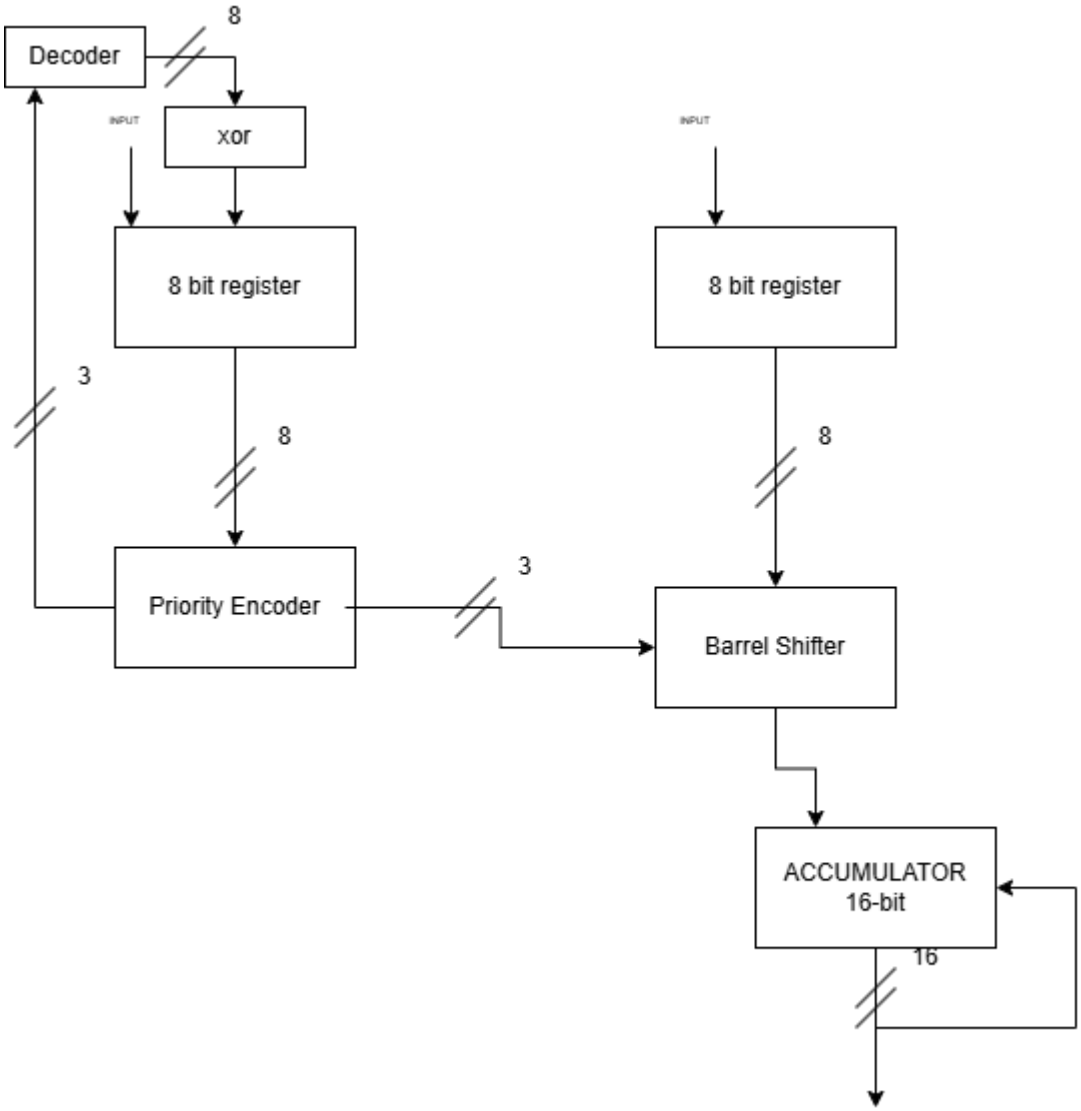
Theory/Description: The circuit is a specialized architecture for high-speed digital multiplication using a Skip-over-Zeros logic (A smart multiplier that saves time by skipping over zeros).

It includes two registers A (which is the multiplier) and B (which is the multiplicand) both of 8-bit in size. It consists a Priority Encoder which identifies the position of the MSB (Most Significant Bit) currently set in register A. A Barrel Shifter receives the position code (sent by the Priority Encoder) which shifts the register B by the corresponding weight. The output is then fed into an 16-bit Accumulator. A Decoder and an XOR gate are used for feedback loop which clears the detected bit in register A, allowing the circuit to process only the non-zero bits of the multiplier, therefore reducing the number of operational cycles.

Reason to reproduce with eSim: The Migration of this architecture to eSim Highlights the capabilities of mixed-signal simulation by using the NgVeri Interface. The implementation utilizes Verilog to model the Priority Encoder, Barrel shifter, Decoder and Accumulator. By using the synthesizeable template, various students can achieve significant educational value by demonstrating that complex designs-originally validated in proprietary tools-can be reproduced successfully using open-source software. It is quite easy to verify the circuit in eSim due to the same mixed signal capabilities and being user friendly.

Expected Outcome/outputs : The aim of the simulation is to verify that the LOD correctly identifies the placement of ones while ignoring/skipping the zeroes thereby reducing the number of clock cycles. The simulation results will be verified by checking them to the expected outcomes of a standard multiplication result and comparing if the circuit actually resulted in reduction of clock cycles which should be less than or equal to the standard 8 cycle multiplier.

Circuit Diagram(s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) : The simulation is expected to show transient waveforms of the multiplication when the calculation is underway. It will also show the partial products generated by the barrel shifter and the overall flow of the calculation, once the multiplier register is rendered zero the multiplication will stop and inform about the calculation being performed successfully by raising a flag meanwhile also indicating that its ready for the next input.

Research Paper/Journal/etc. : Power Efficient Sequential Multiplication Using Pre-computation

Title : Power Efficient Sequential Multiplication Using Pre-computation.
Author : N. Honarmand, M.R.Javaheri, N.Sedaghati-Mokhtari and A. Afzali-Kusha.
Link : lpm_iscas06.pdf

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.