
The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and Simulation of an Efficient 1-bit Low Power **Full Adder** using **GDI** Technique

Theory/Description : The Gate Diffusion Input (GDI) technique is an advanced low-power VLSI design methodology that significantly reduces the complexity of digital circuits compared to traditional Static CMOS and Pass Transistor Logic (PTL). While a standard CMOS 1-bit Full Adder requires 28 transistors to implement the pull-up and pull-down networks, this project utilizes a GDI-based architecture that achieves the same logic functionality using only 10 transistors.

Principle of Operation:

The core of this design is the GDI basic cell, which consists of a simple P-well and N-well CMOS pair. However, unlike standard CMOS where the sources are tied to V_{DD} and Ground, the GDI cell allows three independent inputs:

1. G (Common Gate): Acts as the primary control signal.
2. P (Input to the Source/Drain of PMOS): Can be a signal, VDD, or Ground.
3. N (Input to the Source/Drain of NMOS): Can be a signal, VDD, or Ground.

This flexibility allows a single 2-transistor GDI cell to perform complex functions like XOR, MUX, and AND which would normally require 6-12 transistors in CMOS logic.

Circuit Architecture:

The 1-bit Full Adder is decomposed into two main sub-blocks:

- Sum Generation: This is implemented using two cascaded GDI XOR gates. The first XOR gate computes (A XOR B), and the second XOR gate uses that result and the Carry-in (Cin) to produce the final Sum bit (A XOR B XOR Cin).
- Carry-out (Cout) Generation: The carry signal is generated using a GDI-based 2-to-1 Multiplexer logic. It selects between the input A and Cin based on the intermediate XOR result of (A XOR B).

Key Advantages and Challenges: The primary advantage of this design is a massive reduction in "Power-Delay Product" (PDP) and silicon area. However, GDI logic is known for the "Threshold Voltage Drop" (Vth) effect, where the output voltage might not reach the full rail-to-rail swing. This project uses eSim and Ngspice to analyze these voltage levels and verify that the logic remains robust enough for digital operations in sub-micron technology nodes

Reason to reproduce with eSim :

The reproduction of the "1-bit Low Power GDI Full Adder" using eSim is highly justified due to the following technical and educational factors:

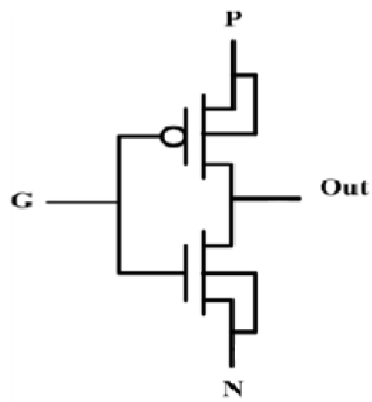
- Open-Source Validation of Advanced Logic: While the original research was likely conducted using proprietary tools like Cadence Virtuoso or Mentor Graphics, migrating it to eSim proves that high-level VLSI research can be accurately reproduced using open-source tools. This supports the global movement toward accessible EDA software.
- Suitability for Transistor-Level Simulation: The Gate Diffusion Input (GDI) technique relies heavily on specific transistor-level behaviors, such as the threshold voltage drop and swing restoration. eSim, with its integrated Ngspice engine, is perfectly suited for this because it allows for precise transient analysis and manual control over MOSFET models (W/L ratios and model parameters), which is essential for verifying GDI logic.
- Educational Value for the VLSI Community: Standard CMOS logic is widely documented, but non-standard logic styles like GDI are rarely found in open-source databases. By reproducing this circuit, I am creating a verified, open-source reference netlist that students and researchers can use to learn about sub-threshold conduction and power-efficient digital design without needing expensive licenses.

- Verification of Low-Power Claims: eSim allows for easy measurement of power dissipation and delay. By migrating this specific design, we can verify the author's claims regarding the "Power-Delay Product" (PDP) reduction in an independent environment, providing a cross-platform verification of the original research results.
- Improvement Over Existing Designs: Most existing full adder projects in the FOSSEE database use conventional 28-transistor CMOS. This migration introduces a 10-transistor alternative, showcasing a significant improvement in silicon area efficiency and static power reduction, which is vital for modern IoT and wearable tech applications.

Expected Outcome/outputs : The expected outcome is a functional simulation showing the digital Sum and Carry outputs for all eight possible input combinations of A, B, and Cin.

The simulation will validate that the 10-transistor count successfully maintains logic levels, even with the inherent threshold voltage drops associated with GDI logic.

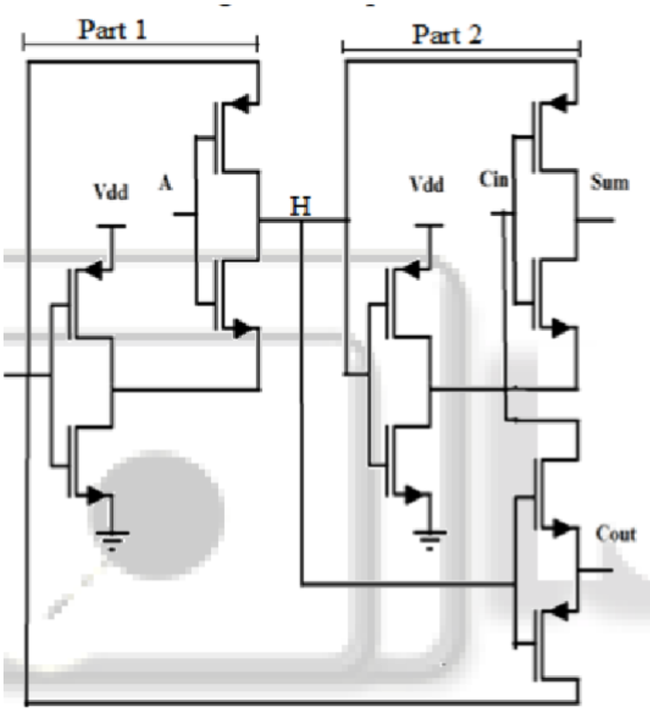
Circuit Diagram(s) :



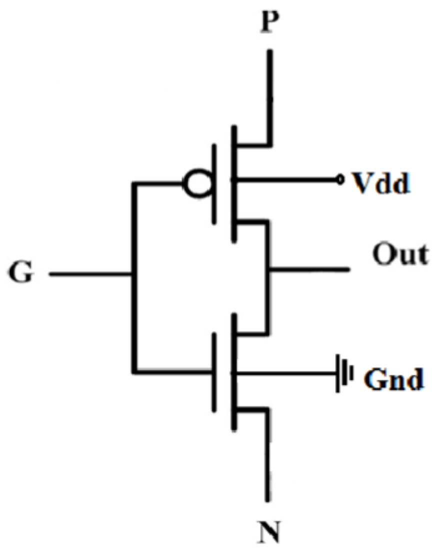
BASIC GDI CIRCUIT

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	NOT
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX

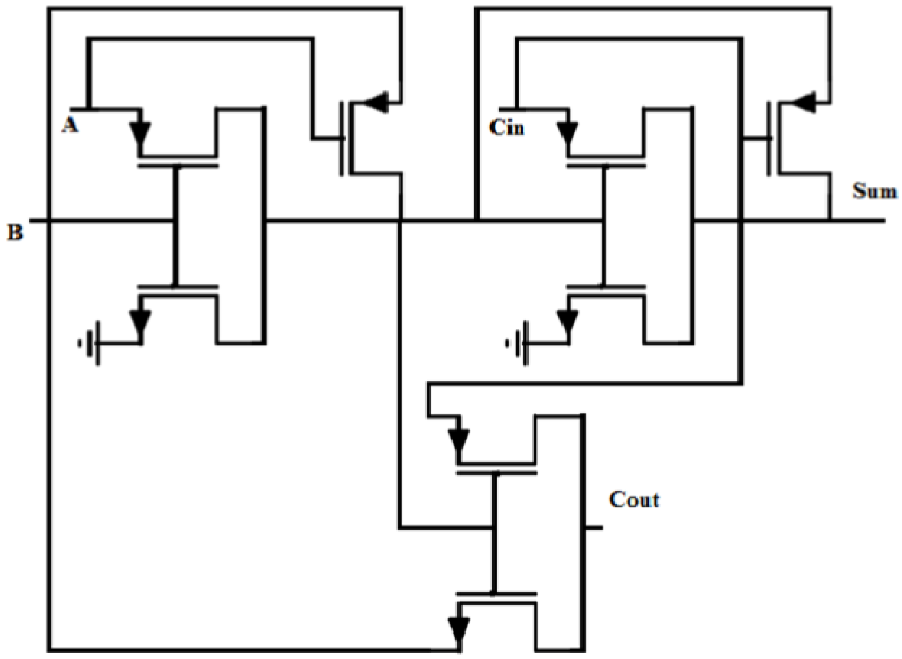
TRUTH TABLE



Design of GDI full adder circuit



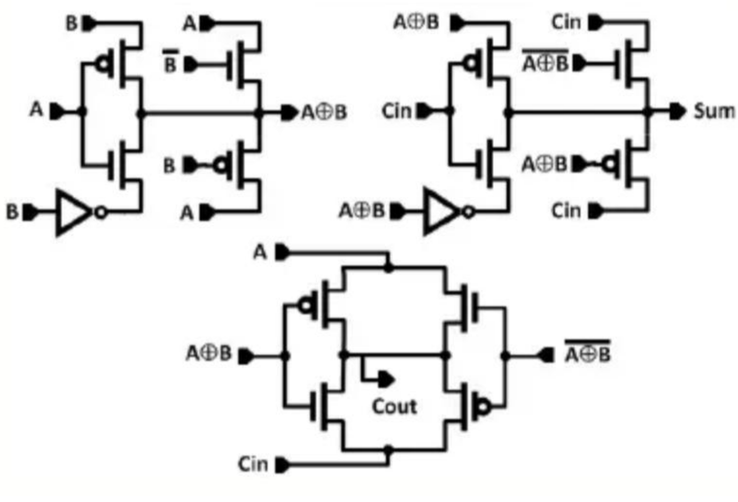
MGDI Cell



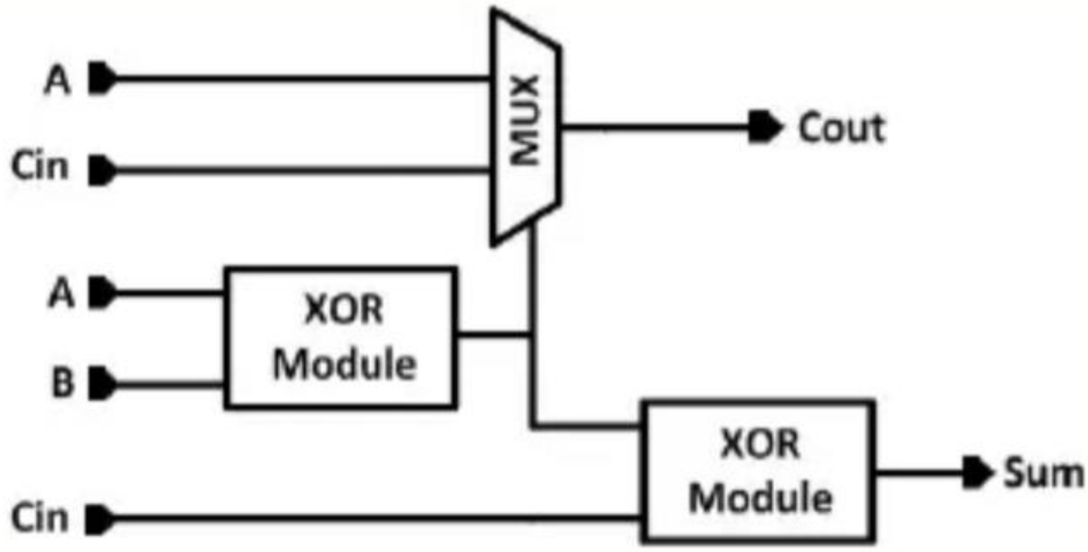
Full adder based on MGDI

- **Modified Gate Diffusion Input (M-GDI)** is one of the most efficient techniques for designing low-power full adders compared to other conventional logic styles reviewed in this study. It effectively achieves significant power minimization while maintaining reduced transistor count and improved performance. Furthermore, the M-GDI technique provides flexibility to implement various full adder architectures, enabling further optimization in terms of power, delay, and area for VLSI applications.

Block Diagram (s) :



Proposed design for 1-Bit Full Adder



Block Diagram For Proposed Full Adder

Expected Results (Input, Output waveforms and/or Multimeter readings) : The transient analysis should show digital pulses for Sum and Cout. Specifically:

- When Inputs (A,B,Cin) are (1,0,0), Sum = 1.8V (High), Cout = 0V (Low).
- When Inputs (A,B,Cin) are (1,1,1), Sum = 1.8V (High), Cout = 1.8V (High).
- Waveforms should demonstrate the truth table of a standard 1-bit Full Adder.

Input Signals and Waveform Shapes:

- Signal Type: Pulse waveforms will be used for all three digital inputs (A, B and Cin) to cover all eight possible logic combinations (000 to 111).
- Input A: Pulse with a period of 40ms and 50% duty cycle.
- Input B: Pulse with a period of 20ms and 50% duty cycle.
- Input Cin: Pulse with a period of 10ms and 50% duty cycle.
- Shape: Rectangular pulses with sharp rise and fall times (e.g., 1ns) to simulate ideal digital transitions.

Voltage Levels:

- Supply Voltage (VDD): 1.8V (assuming a 180nm CMOS technology node).
- Logic High ('1'): Approximately 1.8V. Note that due to the GDI threshold drop (Vth), the output may show levels slightly lower (e.g., 1.5V–1.6V) without buffer restoration.
- Logic Low ('0'): Approximately 0V.

Verification Logic (Truth Table):

Time Interval	A	B	Cin	Sum (Expected)	Cout (Expected)
0–5ms	0	0	0	0V (Low)	0V (Low)
5–10ms	0	0	1	1.8V (High)	0V (Low)
10–15ms	0	1	0	1.8V (High)	0V (Low)
15–20ms	0	1	1	0V (Low)	1.8V (High)
20–25ms	1	0	0	1.8V (High)	0V (Low)
25–30ms	1	0	1	0V (Low)	1.8V (High)
30–35ms	1	1	0	0V (Low)	1.8V (High)
35–40ms	1	1	1	1.8V (High)	1.8V (High)

Performance Metrics:

- Transient Analysis: A simulation run-time of 80ms–100ms will be used to clearly observe multiple cycles of the full adder operation.
- Power Analysis: The average power consumption will be calculated using the .measure command in Ngspice to validate the "Low Power" claim of the GDI technique compared to standard CMOS designs.

Research Paper/Journal/etc. :

Title: Efficient Design of 1-bit Low Power Full Adder using GDI Technique

Author: Deepika Shukla, S.R.P Sinha

Page No.: 2073–2080 (Vol 6, Issue 7)

Link: **https://www.ijsr.net/getabstract.php?paperid=ART20175733**

Source/Reference(s)

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- Pankaj Kumar and Poonam Yadav, "Design and Analysis of GDI Based Full Adder Circuit for Low Power Applications," *IJERA Journal*, Vol. 4, Issue 3. Link: https://www.ijera.com/papers/Vol4_issue3/Version%201/CE4301462465.pdf

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