Design and Implementation of a CMOS Schmitt Trigger using Skywater 130nm

Shravana H S

Department of Electronics and Communication Engineering, Dayananda Sagar Academy of Technology & Management
Bengaluru, Karnataka, India
Email: shravanahs97@gmail.com

***Abstract*-- In this paper, we design and implement a CMOS Schmitt Trigger using the Skywater 130nm PDK technology. The Schmitt Trigger is an electronic circuit known for its ability to filter out noise by employing hysteresis, providing two distinct threshold voltage levels for switching on and off. This dual-threshold feature stabilizes the output by preventing rapid fluctuations when the input signal hovers near the threshold.**

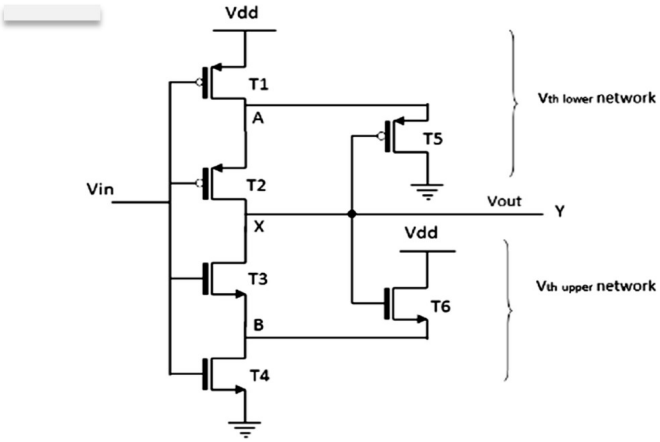
I. INTRODUCTION

The CMOS Schmitt trigger is an essential element in digital circuit design, known for its ability to provide stable output signals in the presence of noisy or slow-changing inputs. Its unique hysteresis property enables the circuit to produce well-defined transitions between high and low states, making it ideal for applications in signal conditioning, waveform shaping, and pulse generation. This paper will explore the implementation considerations, and the practical realization of the circuit using CMOS technology. Additionally, we will discuss its significance in enhancing the performance and reliability of digital systems.

II. DESIGN PRINCIPLE

A Schmitt trigger has two output stages, providing a stable high output only when the input voltage exceeds the upper reference voltage +Vth. Conversely, the output is low (or 0) when the input voltage falls below the lower reference voltage -Vth This hysteresis effect allows the Schmitt trigger to maintain its output state even in the presence of noise, ensuring reliable signal transitions.

III. IMPLEMENTATION



The CMOS Schmitt trigger uses a pull-up network of PMOS transistors (T1 and T2) and a pull-down network of NMOS transistors (T3 and T4) to establish distinct upper and lower switching thresholds, creating hysteresis. The pull-up network pulls the output high when the input exceeds the upper threshold voltage (+Vth), while the pull-down network pulls it low when it falls below the lower threshold voltage (-Vth). Additional NMOS and PMOS transistors help generate +Vcc when the input is high and 0V when it is low, allowing for precise control of switching and ensuring stable transitions with effective hysteresis.

V. CONCLUSION

This design ensures reliable performance in noise-prone environments, making it ideal for applications requiring precise and stable signal processing.

VI. REFERENCES

- S. K. Jha, P. Verma, and M. Taleja, "Design of low power CMOS based Schmitt trigger in 180nm technology," University School of Information, Delhi, India, 2021.
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