Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Simulation of an Ultra-Compact Leaky Integrate-and-Fire Neuron Circuit Using eSim

Theory/Description : Biological neurons communicate by generating voltage spikes when their membrane potential crosses a firing threshold. The leaky integrate-and-fire (LIF) model captures this by treating the neuron membrane as a capacitor that charges under an input stimulus, leaks through a parallel resistor, and fires when the voltage reaches a critical threshold. Stoliar et al. (2020) demonstrated that a single Silicon Controlled Rectifier (SCR), one resistor, and one capacitor form an ultra-compact analog circuit that faithfully replicates this behavior. The SCR acts as the threshold-and-reset element: it remains non-conducting while VMEM is below the holding voltage, then triggers and rapidly discharges the capacitor once threshold is exceeded, producing a spike at VOUT. Figure 1 of the paper validates this circuit by demonstrating two key neuro-computational properties — threshold detection (no spiking below a critical VIN) and rate coding (spiking frequency increases with VIN amplitude) — through excellent agreement between measured hardware data and simulation.

Reason to reproduce with eSim : The UCN circuit from Stoliar et al. (2020) was originally simulated using commercial SPICE tools, and migrating it to eSim creates an open-source reference implementation for the neuromorphic design community. Reproducing this circuit in eSim also validates the platform's capability for analog neuron circuit simulation, contributing directly to the open-source resource database of the Research Migration Project.

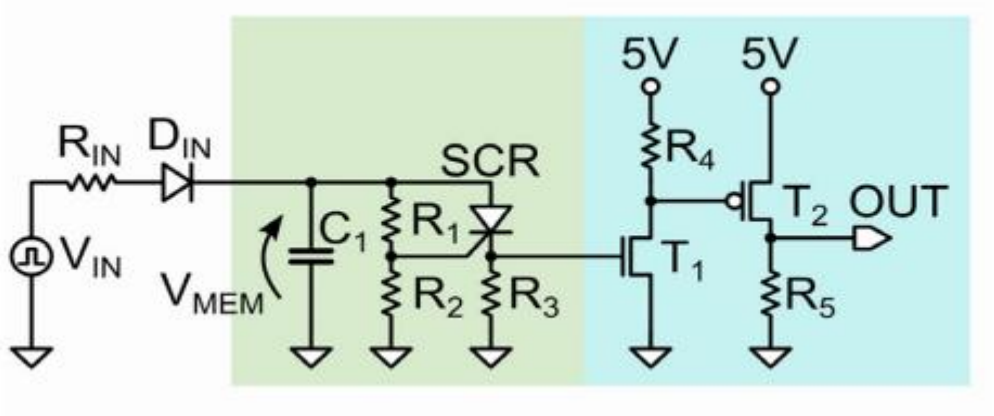
Expected Outcome/outputs : Transient simulation of the basic UCN circuit under voltage pulse inputs of varying amplitude is expected to produce three observable behaviours:

- **Threshold detection — Below a critical VIN, VMEM charges but never triggers the SCR and no spike appears at VOUT. Above it, VMEM crosses the holding voltage, the**

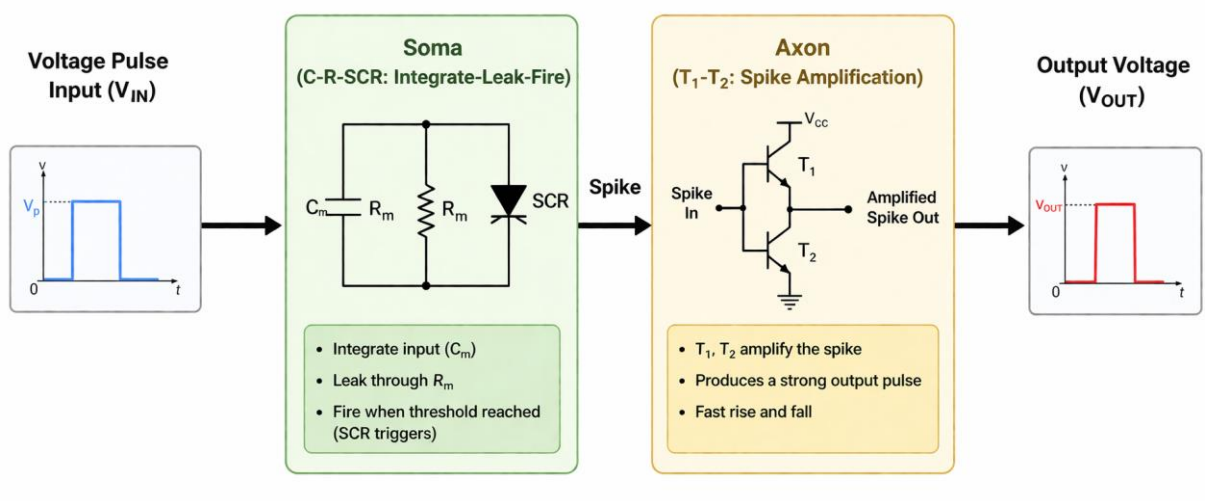
capacitor resets, and a spike is produced. The threshold VIN value will be identified from the simulation.

- **Rate coding — As VIN increases beyond threshold, spiking frequency at VOUT increases proportionally, demonstrating that the circuit encodes input intensity as spike frequency.**
- **VMEM dynamics — The VMEM trace will show integration (charging), leak (RC decay below threshold), and reset (sharp drop after each spike), confirming correct LIF behaviour.**

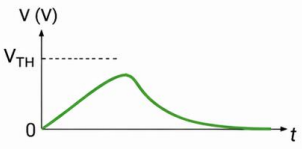
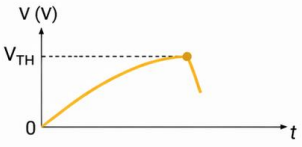
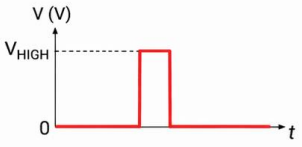
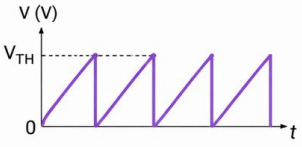
Circuit Diagram(s) : The circuit consists of a voltage pulse input, a membrane capacitor, a leak resistor, an SCR-based threshold element, and an output transistor stage. The capacitor and resistor form the soma section, while the transistor stage represents the axon output. The complete schematic is reproduced in eSim as shown in the attached figure.

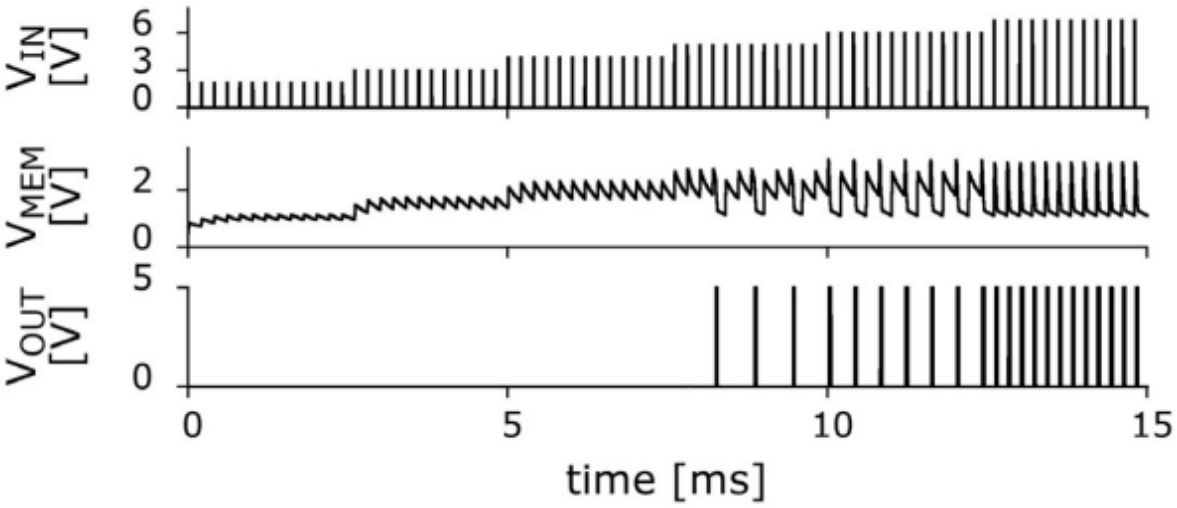


Block Diagram (s) : The block diagram shows voltage pulse input to the soma section (C-R-SCR for integrate-leak-fire) and then to the axon section (T1-T2 for spike amplification), producing the output VOUT spike. The attached figure shows the complete signal flow.



Expected Results (Input, Output waveforms and/or Multimeter readings) : Expected VIN, VMEM, and VOUT waveforms from eSim simulation (across multiple pulse amplitudes) are shown below for comparison against the simulated panel of Figure 1 from Stoliar et al. (2020). The simulation should reproduce threshold detection and rate-coding behavior with excellent agreement.

V_{IN} Amplitude	V_{MEM}	V_{OUT}	Derivation
Below threshold (~0.3 V)	**Partial charge, leaks back** 	**No spike** 	**RC leak dynamics** $V_{MEM}(t) = V_{IN}(1 - e^{-t/RC})e^{-t/RC}$ Leaky integration below threshold
At threshold (~0.5 V)	**Reaches threshold with transient** 	**Single spike** 	**Threshold V_{IN} identified** V_{MEM} reaches V_{TH} → SCR triggers → single spike
Above threshold (~0.7 V)	**Periodic charge-reset** 	**Regular spikes** 	**Rate coding confirmed** $f_{spike} \approx \frac{1}{\tau_{charge} + \tau_{reset}}$ Higher V_{IN} → higher rate



Research Paper/Journal/etc. :

Title : Biologically Relevant Dynamical Behaviors Realized in an Ultra-Compact Neuron Model

Author : Pablo Stoliar, Olivier Schneegans, Marcelo J. Rozenberg
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Link :
https://www.frontiersin.org/journals/neuroscience/articles/10.3389/fnins.2020.00421/full

1. **Source/Reference(s) : Stoliar P., Schneegans O., Rozenberg M.J. — *Frontiers in Neuroscience*, 14:421, 2020 *(primary)***
2. **Rozenberg M.J., Schneegans O., Stoliar P. — "An ultra-compact leaky-integrate-and-fire model for building spiking neural networks," *Scientific Reports*, 9:11123, 2019 *(Figure 1 originates here)***
3. **EC103D1 SCR SPICE Model — Littelfuse Inc. (https://www.littelfuse.com/~/media/electronics/datasheets/thyristors/littelfuse/thyristor_datasheet_ec103d1.pdf)**
4. **Izhikevich E.M. — "Which model to use for cortical spiking neurons?" *IEEE Transactions on Neural Networks*, 15(5):1063-1070, 2004**
5. **eSim User Manual v2.4 — FOSSEE, IIT Bombay (https://esim.fossee.in/downloads.html)**
