Research Migration Project Proposal

JK Master-Slave Flip-Flop and Removal of Race Around Condition

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Title of the circuit
JK Master-Slave Flip-Flop for Elimination of Race Around Condition

Theory / Description
The **JK Master-Slave Flip-Flop** is a clocked sequential logic circuit designed to store one bit of binary information while eliminating the **race-around condition** present in a conventional JK flip-flop.

A basic JK flip-flop is an improved form of the SR flip-flop in which the invalid state is removed. Its operation depends on the inputs **J** and **K** along with the clock signal. When both inputs are high ($J = K = 1$), the output toggles its state. However, if the clock pulse width is greater than the propagation delay of the flip-flop, the output may toggle continuously within the same clock pulse. This repeated toggling is known as the **race-around condition**, leading to an unpredictable final output.

To overcome this problem, the **master-slave configuration** is used. It consists of two level-sensitive latches connected in series:

- **Master latch**
- **Slave latch**

The master latch is enabled during the **HIGH level of the clock pulse**, while the slave latch is enabled during the **LOW level of the clock pulse** through an inverted clock.

This arrangement ensures that the input is first captured by the master stage and then transferred to the slave stage only after the clock transitions. As a result, the output changes **only once per complete clock cycle**, even when $J = K = 1$.

Hence, the master-slave JK flip-flop successfully eliminates the race-around condition and provides stable and predictable output transitions, making it highly useful in **counters, shift registers, memory elements, and synchronous sequential circuits**.

Reason to reproduce with eSim

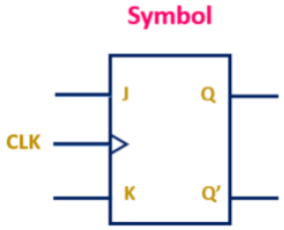
The primary reason for using eSim is that the objective of this project is not only to simulate the circuit but also to **migrate digital circuit designs from proprietary tools to an open-source ecosystem**. Since many commercial simulation tools require paid licenses and have restricted access, eSim provides a cost-effective and accessible alternative for students and researchers.

For the **JK Master-Slave Flip-Flop**, eSim is particularly suitable because it allows:

- **easy schematic capture**
- digital and mixed-signal simulation support
- waveform visualization for clock and output transitions
- verification of timing behavior
- open-source reproducibility for academic use

Expected Outcome / Outputs

The output should toggle once per clock cycle for J = K = 1 without multiple transitions within the same pulse.



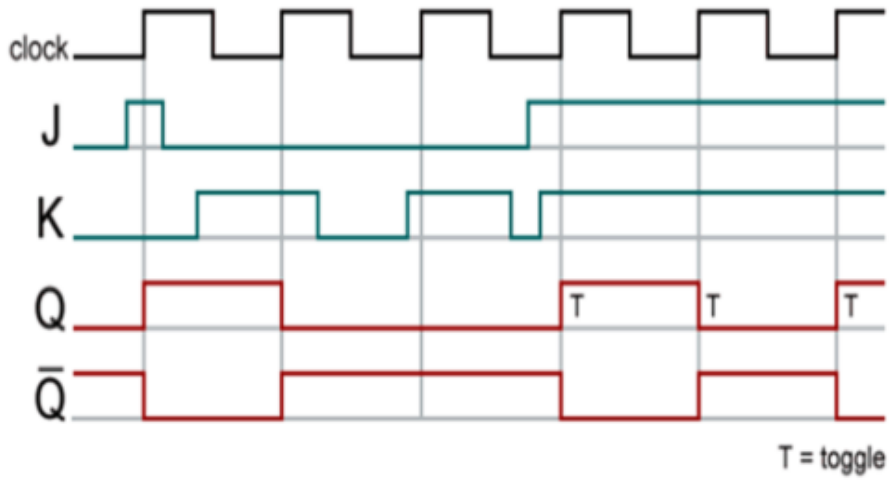
Truth Table

CLK	J	K	Q_{n+1}
↑	0	0	Q_n
↑	0	1	0
↑	1	0	1
↑	1	1	Q_n'

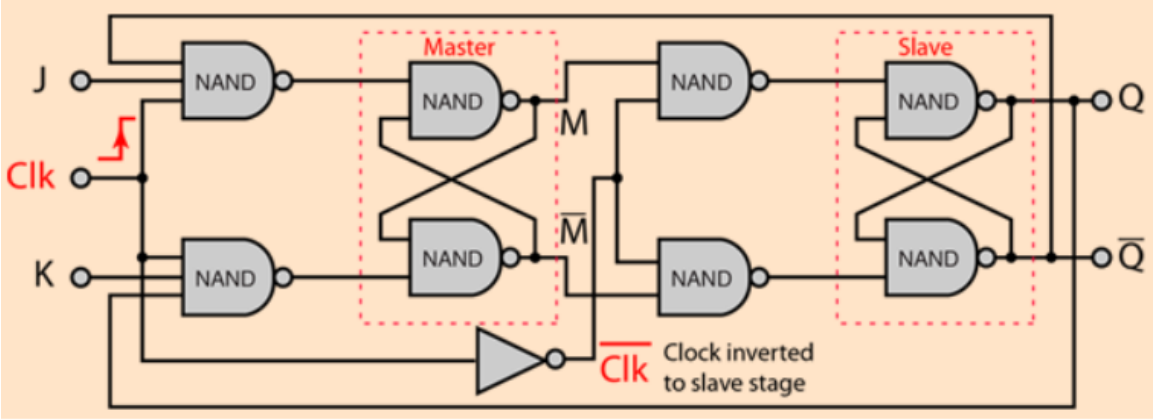
JK Flip-Flop Symbol and Truth Table

Expected Results:

Q should toggle once for every complete clock pulse when J and K both are HIGH(1).



Circuit Diagram:



Master Slave JK Flip Flop

References:

Title : Master-Slave JK Flip Flop

Author : Geeks for Geeks.
Link : (Direct link to IEEE / Scopus / Google Scholar / Patent source)

Title : N-MOS JK MASTER/SLAVE FLIP FLOP DESIGN FOR USE IN HIGH SPEED CONTROL AND COUNTING APPLICATIONS
Author : ASHOK SRIVASTAVA

Link : (Direct link to IEEE / Scopus / Google Scholar / Patent source)