Research Migration Project

https://esim.fossee.in/research-migration-project

Name of the participant : DAPHNE STARINA J

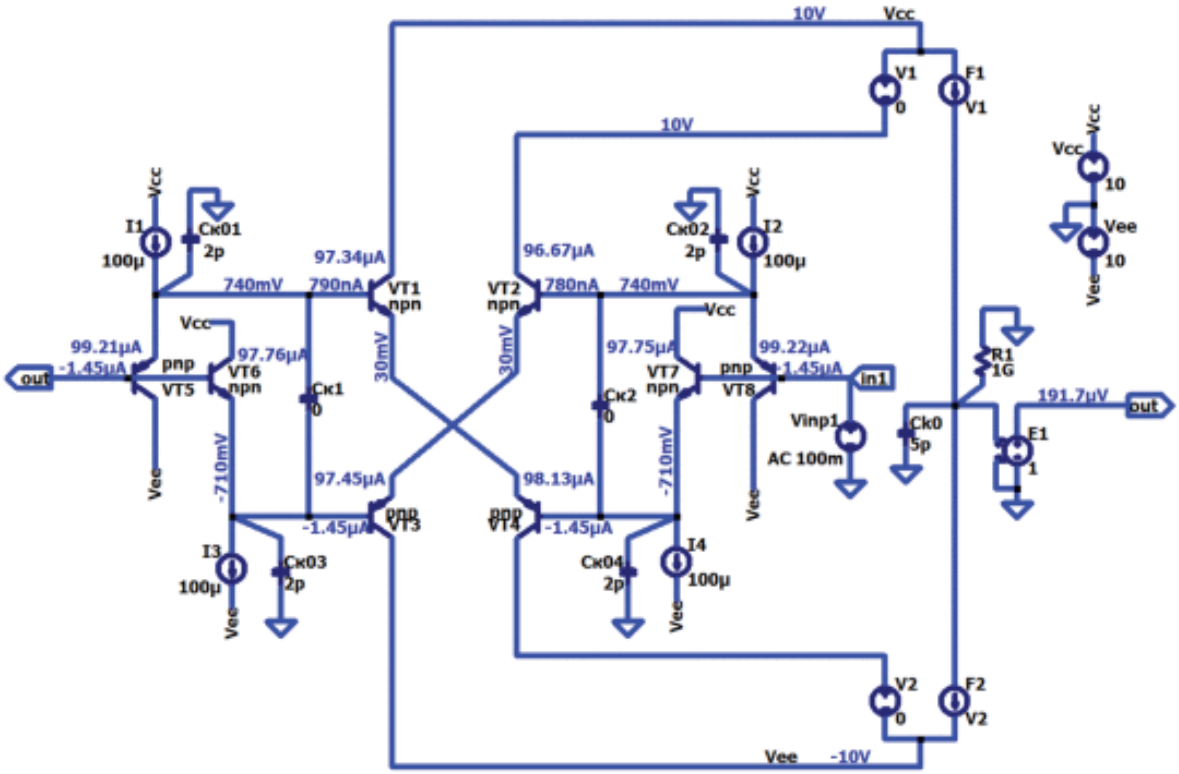
Institution : Department of Electronics and Instrumentation Engineering, Madras Institute of Technology ,Anna University ,Chennai, Tamil Nadu, India.

Title of the circuit : High-Speed Operational Amplifier with Differentiating Transient Correction Circuits

Theory/Description :

This project proposes the implementation of a high-speed operational amplifier (OpAmp)using differentiating transient correction circuits. The design is based on a two-stage operational amplifier architecture consisting of a differential input stage, current mirrors, compensation circuitry, and an output buffer stage. The proposed IEEE design improves the dynamic response of the Op-Amp by introducing differentiating correction capacitors in the internal nodes of the circuit. These correction capacitors inject additional transient current during switching events, thereby accelerating the charging and discharging of internal parasitic capacitances. As a result, the output transition becomes significantly faster without increasing the static power consumption of the amplifier.The circuit mainly consists of Differential input transistor stage, Current mirror biasing circuits,Integrating compensation capacitor for stability,Differentiating correction capacitors for transient enhancement,Output buffer stage.

Circuit Diagram:



Reason to reproduce with eSim :

Reproducing this circuit in eSim is useful for validating a research-level analog design in an open-source simulation environment. The original work was modeled in LTspice, and migrating it into eSim using Ngspice will help demonstrate the capability of eSim in handling advanced analog IC circuits.

Expected Outcome/outputs :

1. Improved Slew Rate: The output voltage is expected to exhibit a significantly faster rise and fall time compared to the conventional Op-Amp design.

2. Transient Response Enhancement: The waveform will show sharper output transitions due to the differentiating correction capacitors introduced in the internal nodes.

Expected Results (Input, Output waveforms and/or Multimeter readings) :

1. Input Signal: A step input voltage pulse will be applied to the amplifier input to observe transient performance.
2. Output Waveform: The output waveform is expected to rise and fall rapidly with significantly reduced transition delay.
3. Slew Rate Measurement: The output slope is expected to improve substantially when differentiating capacitors are included.
4. Frequency Characteristics: AC analysis is expected to show high open-loop gain and wide bandwidth.
5. Comparative Observation: The output response without correction capacitors will show slower transitions, while the corrected circuit will show faster edge response

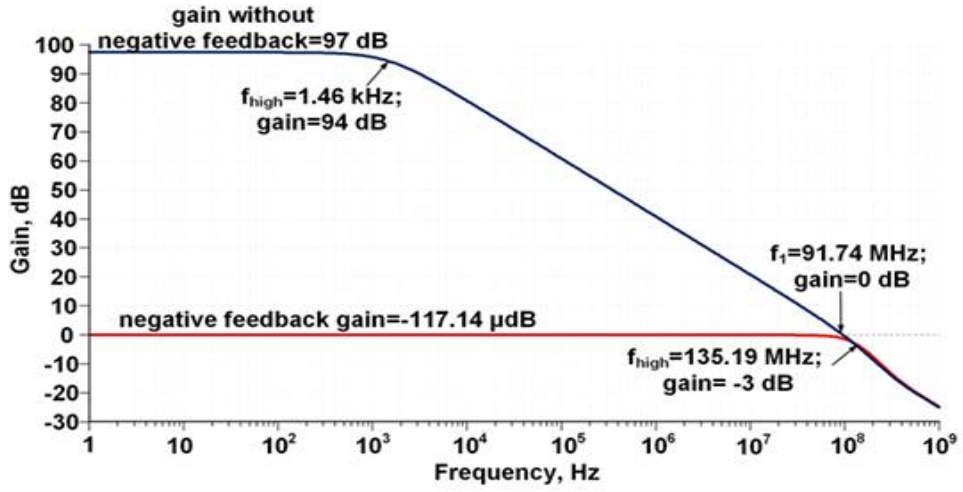


Fig. 6. LAFR of coefficients gain of open-loop and close-loop Op-Amp on Fig. 5.

Research Paper/Journal:

Title: High-Speed Operational Amplifier with Differentiating Transient Correction Circuits

Link:[High-Speed Operational Amplifier with Differentiating Transient Correction Circuits | IEEE Conference Publication | IEEE Xplore]

Authors: Nikolay N. Prokopenko, Oleg V. Dvornikov, Alexey A. Zhuk

Source / References:

IEEE Conference Paper (SIBCON 2022)