

Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : Prashant Kumar Garg

Affiliation / Institution : Department of Electronics and Communication Engineering , Jaypee Institute of Information Technology, Sec-62, Noida, UttarPradesh

Title of the circuit : Design and Simulation of Cascaded hybrid amplifier using CS-CE Amplifier to gain high voltage Gain.

Theory/Description :

A hybrid cascade amplifier combines a MOSFET-based **Common Source** (CS) stage with a BJT-based **Common Emitter** (CE) stage to achieve high voltage gain.

The CS stage provides **high input impedance** and initial voltage amplification using an N-channel MOSFET biased by a voltage divider (RG1, RG2). The drain resistor RD and source resistor RS set the DC operating point.

The CE stage provides additional **voltage amplification** using BC547 NPN transistor biased by R3 and R4 voltage divider. The emitter bypass capacitor CE maximizes AC gain.

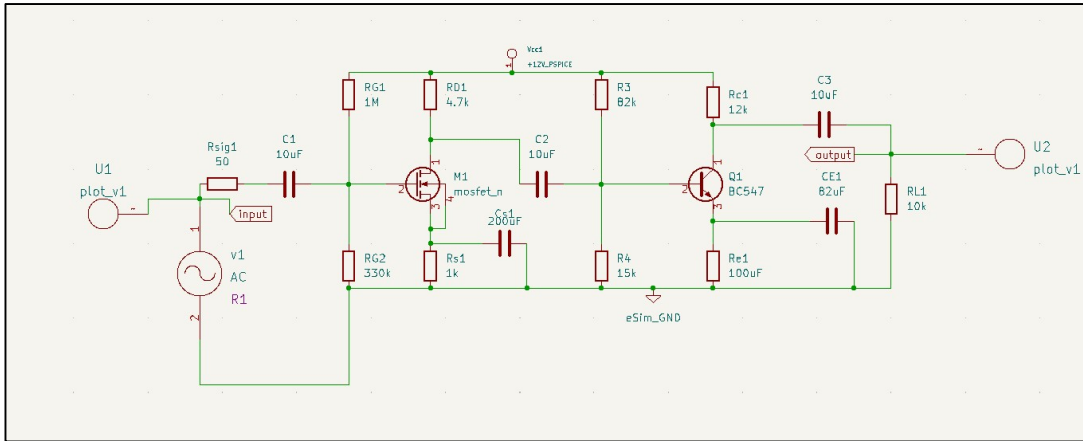
Both stages are AC coupled via capacitors C1, C2, C3 to block DC while passing AC signals.

Total **theoretical voltage gain** = $Av1 \times Av2 \approx 500$.

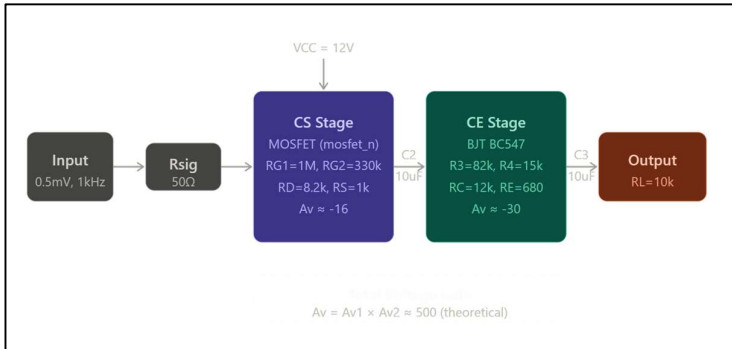
Expected Outcome/outputs :

1. Input: Sinusoidal signal of 0.5mV amplitude at 1kHz
2. Output: Amplified sinusoidal signal with: - Voltage gain ≈ 5 (simulated), ~ 500 (theoretical)
3. Frequency response: Good amplification at 1kHz midband

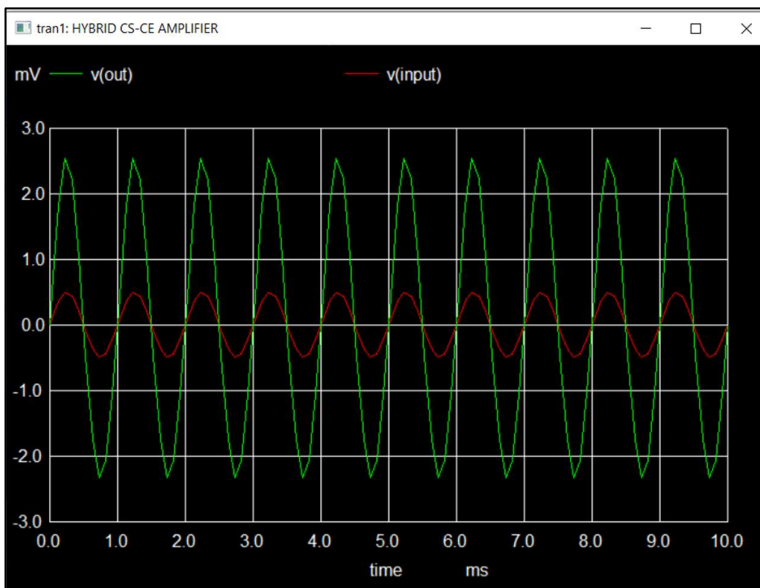
Circuit Diagram(s) :



Block Diagram (s) : (Include a high-level block diagram showing major functional blocks and signal flow. This helps in understanding the system architecture before detailed implementation.)



Expected Results (Input, Output waveforms and/or Multimeter readings) :



Source/Reference(s) :

1. Sedra & Smith, Microelectronic Circuits, Oxford University Press.
 2. Razavi, Design of Analog CMOS Integrated Circuits.
 3. <https://ngspice.sourceforge.io/>
 4. <https://esim.fossee.in/>
-