Research Migration Project

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Title of the circuit : Design and Simulation of a VCO-Based Analog-to-Digital Converter Using Time-Domain Conversion

Description: The proposed circuit implements a time-domain Analog-to-Digital Converter (ADC) using a Voltage-Controlled Oscillator (VCO). The input analog voltage controls the oscillation frequency of the VCO, such that higher input voltages produce higher oscillation frequencies.

The oscillator output is passed through a buffer stage to ensure clean digital transitions and proper logic levels. This conditioned signal is then applied to a digital counter, which counts the number of oscillations within a fixed observation interval. The counted value is proportional to the input voltage and represents its digital equivalent.

To restrict counting to a defined duration, a control signal is used to create a sampling window, ensuring consistent measurement. Since the counter output continuously changes, a latch is used to capture and hold the final count value at the end of this interval, providing a stable output.

Thus, the system performs conversion through voltage-to-frequency conversion, frequency-to-digital counting, and output stabilization, forming a simple and effective time-domain ADC architecture.

Reason to reproduce with eSim :

The proposed VCO-based Analog-to-Digital Converter is well-suited for implementation using eSim due to its combination of analog and digital building blocks, making it ideal for mixed-signal simulation. eSim provides an open-source platform that allows accurate modeling of components such as oscillators, logic gates, counters, and latches within a single environment.

This circuit offers strong educational value as it demonstrates the practical realization of time-domain conversion techniques, helping to bridge the gap between analog and digital design concepts. The step-by-step simulation enables easy verification of each stage, including voltage-to-frequency conversion, pulse counting, and output stabilization.

Additionally, eSim allows flexibility in modifying parameters such as input voltage, timing intervals, and circuit configurations, enabling performance analysis and optimization. This makes it an effective tool for understanding system behavior and validating the design without the need for physical hardware.

Expected Outcome/outputs : Upon simulation, the circuit is expected to demonstrate a clear relationship between the input analog voltage and the digital output. As the input voltage

increases, the frequency of the VCO output should increase proportionally, resulting in a higher number of pulses within the observation interval.

The digital counter will produce a corresponding binary count (Q0–Q3), representing the number of oscillations detected during the sampling window. Lower input voltages will result in smaller counts, while higher input voltages will produce larger counts, effectively quantizing the analog input into discrete digital levels.

The latch will capture and hold the final counter value at the end of the observation period, ensuring a stable and readable digital output. The output should remain constant until the next sampling cycle.

Performance can be validated by observing waveforms at different stages, including the VCO output, counter transitions, and latched output. A monotonic increase in digital output with respect to input voltage confirms correct operation. The system should demonstrate consistent behavior across simulations with varying input values and timing conditions.

Circuit Diagram(s) : The overall system is divided into multiple stages, where each stage performs a specific function in the analog-to-digital conversion process.

Stage 1: Voltage-Controlled Oscillator (VCO)

The input analog voltage (VIN) is applied to the VCO. This block converts the input voltage into a frequency signal. As VIN increases, the oscillation frequency increases, and as VIN decreases, the frequency reduces. This stage performs voltage-to-frequency conversion.

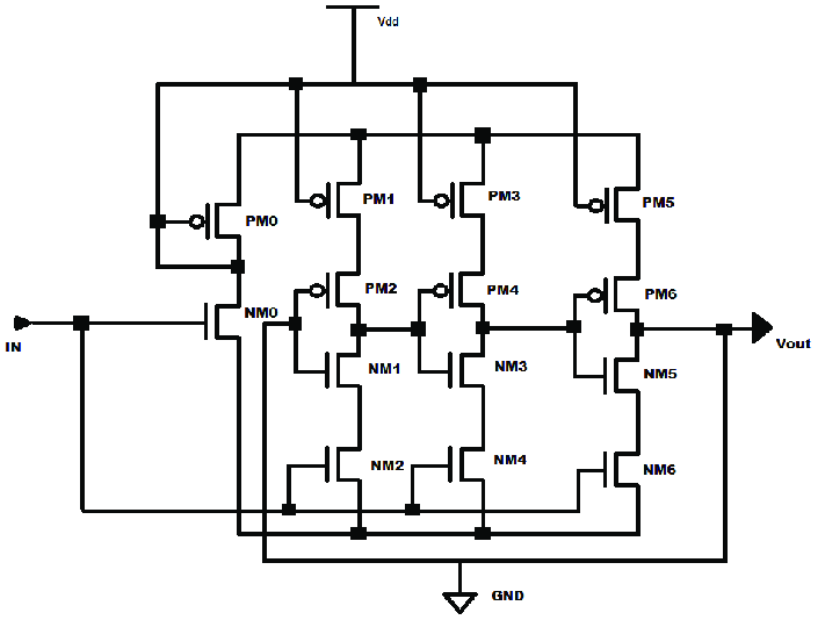


Fig: Schematic of 3-stage current starved VCO

Stage 2: Buffer Stage

The output of the VCO is passed through a buffer consisting of cascaded inverters. This stage improves signal quality by sharpening rise and fall times and ensuring full logic levels, making the signal suitable for digital processing.

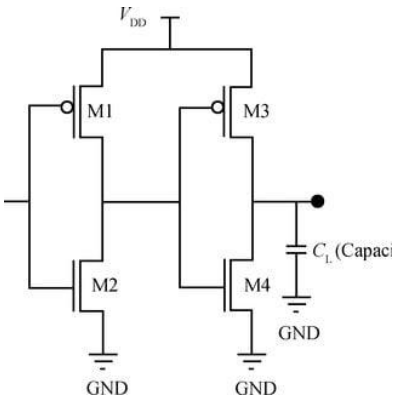


Fig: CMOS buffer circuit

Stage 3: Sampling Window

A control signal is used to define a fixed time interval during which the signal is allowed to pass. This is implemented using gating logic (AND gate). Only during this window are the oscillator pulses allowed to reach the counter, ensuring consistent measurement.

Stage 4: Counter

The gated signal is applied to a 4-bit counter built using flip-flops. The counter increments with each incoming pulse and produces a binary output (Q0–Q3). The total count represents the number of oscillations within the sampling window.

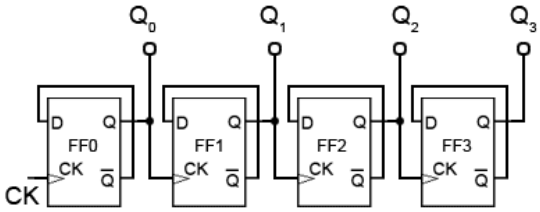


Fig: 4-bit Asynchronous Counter

Stage 5: Latch (Output Storage)

At the end of the sampling interval, a latch captures the counter output and holds it constant. This prevents continuous changes in output and provides a stable digital representation of the input voltage.

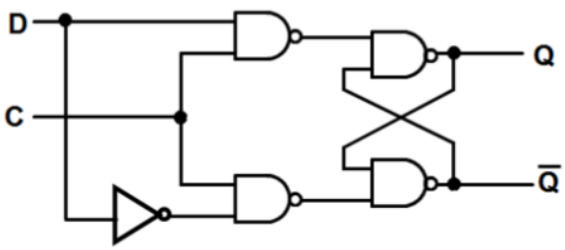
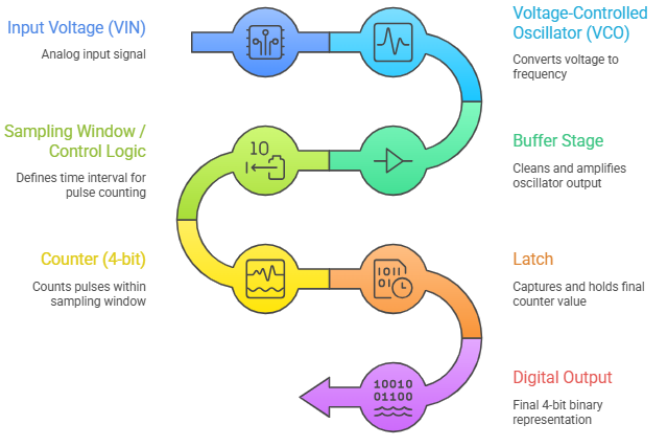


Fig: schematic of D-latch

Stage 6: Digital Output
The final output is a 4-bit binary value corresponding to the input analog voltage. Higher input voltages result in higher counts, demonstrating successful analog-to-digital conversion.

Thus, the system operates sequentially by converting voltage to frequency, frequency to count, and finally storing the result as a stable digital output.

Block Diagram:



Expected Results: The input to the circuit is a DC analog voltage (VIN), which can be varied within the operating range (e.g., 0–5 V). This input controls the frequency of the VCO. At lower input voltages, the VCO produces a low-frequency waveform, while higher input voltages result in higher frequency oscillations.

The output of the VCO, observed on the waveform viewer, is a periodic pulse signal whose frequency varies with VIN. After passing through the buffer stage, the waveform becomes a clean square wave with sharp transitions and full logic levels (0 to VDD).

At the counter output (Q0–Q3), digital waveforms are observed, representing binary counting sequences. The counting rate increases with increasing input voltage. During the sampling window, the counter increments, and after the window ends, the latch holds the final binary value constant.

The final output is a stable 4-bit digital signal corresponding to the input voltage level. For example, lower input voltages may produce outputs like 0001 or 0010, while higher voltages may result in outputs such as 1010 or higher.

Multimeter readings can be used to verify DC levels (e.g., VIN and logic levels at outputs), while waveform analysis confirms the relationship between input voltage, oscillation frequency, and digital count. A consistent increase in output count with increasing VIN validates correct circuit operation.

Research Paper/Journal/etc. :
Title: *A Time-to-Digital Converter-Based Analog-to-Digital Converter*
Author: J. Kim, S. Lee, and K. Lee
Link: IEEE Xplore Document

Title: *Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter*
Author: J. Kim, T.-K. Jang, Y.-G. Yoon, and S. Cho
Link: IEEE Xplore Document

Source/Reference(s) :

- Phillip E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press.
- Marcel J.M. Pelgrom, *Analog-to-Digital Conversion*, Springer.
- Time-Based ADC Overview (Analog Devices)
- ADC Basics Application Note (Texas Instruments)
