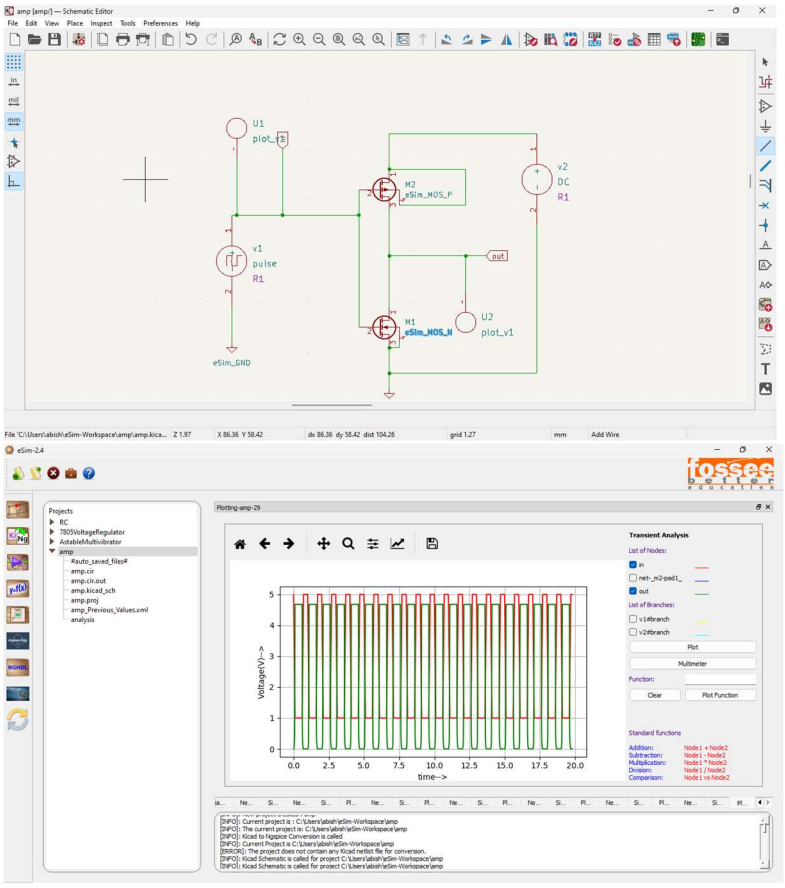
NOT GATE (CMOS)

Problem Statement:

Design a CMOS NOT gate using standard CMOS technology to perform logical inversion of the input signal. The circuit should ensure low power consumption, high speed, and proper noise margins. Use a specified process node (e.g., 90nm or 180nm) and validate the design through transient analysis. Analyze the input-output characteristics, propagation delay, and power dissipation. Ensure the design meets the functional and performance requirements.

Solution :



Reference :

https://www.elprocus.com/cmos-inverter/