Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : Vadla Bhavya
Institution : BVRIT Hyderabad College of Engineering for Women.

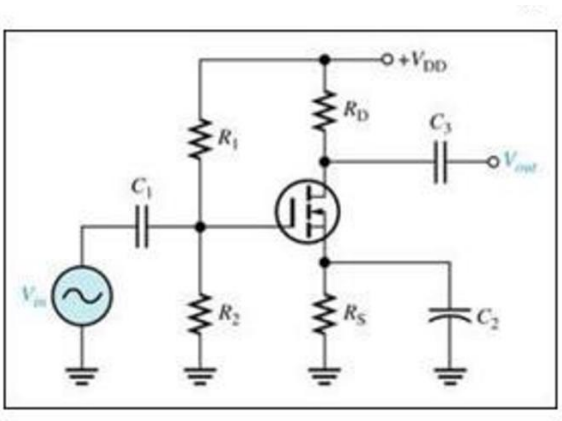
Title of the circuit : Design and Performance Analysis of a Common Source MOSFET Amplifier Using eSim

Theory: The Common Source (CS) MOSFET amplifier is a fundamental analog amplifier configuration widely used in signal processing and integrated circuit design. In this configuration, the source terminal of the MOSFET is common to both input and output terminals. The input signal is applied at the gate, and the output is obtained from the drain. The biasing network ensures that the MOSFET operates in the saturation region for proper amplification. The voltage gain of the amplifier is approximately: Av ≈ −gm × RD Where, gm is the transconductance of the MOSFET.

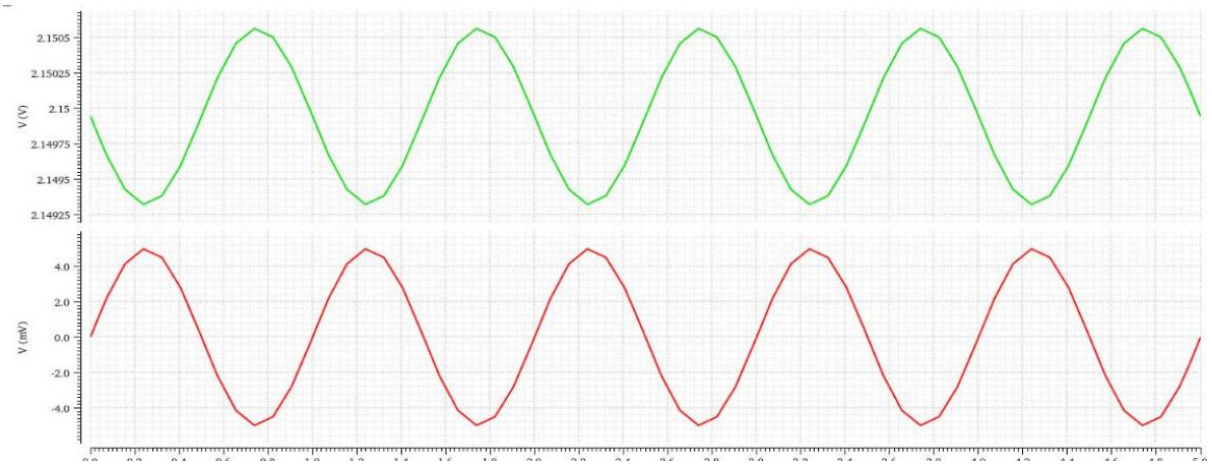
Expected Outcome:

- Proper DC biasing of MOSFET in saturation region.
- Stable Q-point (VDS > VGS − VT).
- Amplified output waveform.
- 180° phase shift between input and output.
- Measurable voltage gain.
- Observation of drain current and power dissipation.

Circuit Diagram :



Expected Results:



Source/Reference(s) :

1. Sedra & Smith, Microelectronic Circuits, Oxford University Press.

2. Razavi, Design of Analog CMOS Integrated Circuits.

3. Low Power Common Source Amplifier Design For Analog Signal Processing Applications, IJCRT Journal.

4. https://ngspice.sourceforge.io/

5. https://esim.fossee.in/