Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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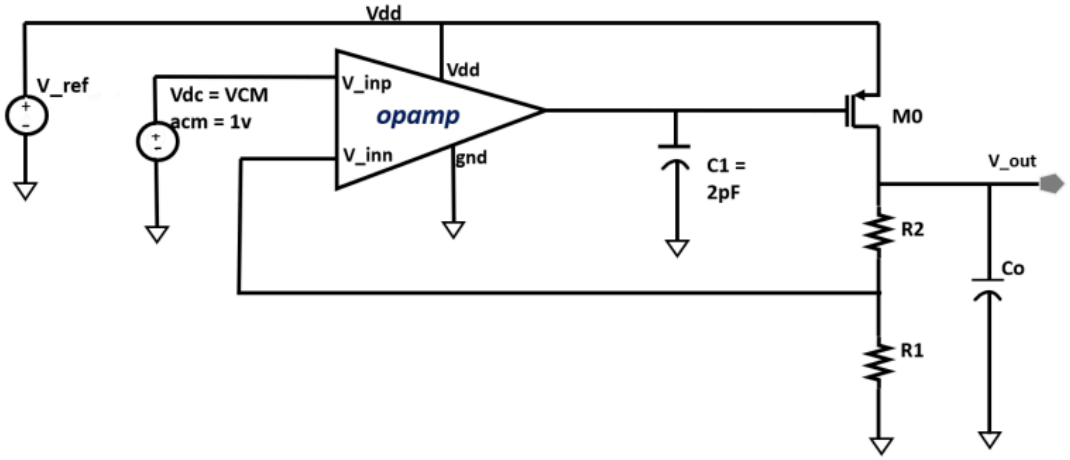
Title of the circuit : Simulation of a CMOS Low Dropout Voltage Regulator

Theory/Description : A Low Dropout Voltage Regulator (LDO) is a commonly used linear power supply circuit that provides a stable output voltage even when the input voltage is only slightly higher than the desired output.The proposed circuit is a CMOS-based LDO designed using 180 nm technology. It mainly consists of an error amplifier, a PMOS pass transistor, a resistive feedback network, and an output load capacitor. The error amplifier continuously compares the feedback voltage derived from the output with a reference voltage and adjusts the gate voltage of the pass transistor accordingly. This negative feedback mechanism helps maintain a constant output voltage despite changes in input supply or load current.

Reason to reproduce with eSim : The CMOS LDO voltage regulator selected for this work was originally designed and verified using Cadence Virtuoso tool. By recreating the same circuit in eSim, the design can be studied and validated using an open-source simulation platform.

Expected Outcome/outputs : Upon simulation in eSim, the LDO regulator is expected to produce a stable regulated output voltage close to the value reported in the reference paper. The performance of the circuit will be validated through line regulation, load regulation, and transient response simulations. The output voltage behavior under step changes in load current and supply voltage will be observed and compared with the published results.

Circuit Diagram(s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) : The expected results include DC output voltage regulation plots, transient response waveforms showing output stability during load variations, and voltage measurements demonstrating line and load regulation. These results will be compared qualitatively with those reported in the reference publication.

Research Paper/Journal/etc. : R. M. R and A. V. R, "Design of a Low Dropout Voltage Regulator (LDO) Using SCL 180nm CMOS Technology," 2024 International Conference on Smart Electronics and Communication Systems (ISENSE), Kottayam, India, 2024, pp. 1-5, doi: 10.1109/ISENSE63713.2024.10872390. keywords: {Temperature distribution;Regulators;Linearity;CMOS technology;Stability analysis;Manufacturing;Transistors;Voltage control;Integrated circuit reliability;Thermal stability;Low Dropout Regulator (LDO);SCL 180nm CMOS Technology;Power Management;gm/Id Methodology;Corner Analysis;voltage regulator},

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Source/Reference(s) : Adel S. Sedra, Kenneth C. Smith & Arun N. Chandorkar, Microelectronic Circuits, Theory and Application.
