The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : V.PRAJEEN

Affiliation / Institution : Department Of Electronics and communication Engineering , Meenakshi Sundararajan Engineering College , Chennai

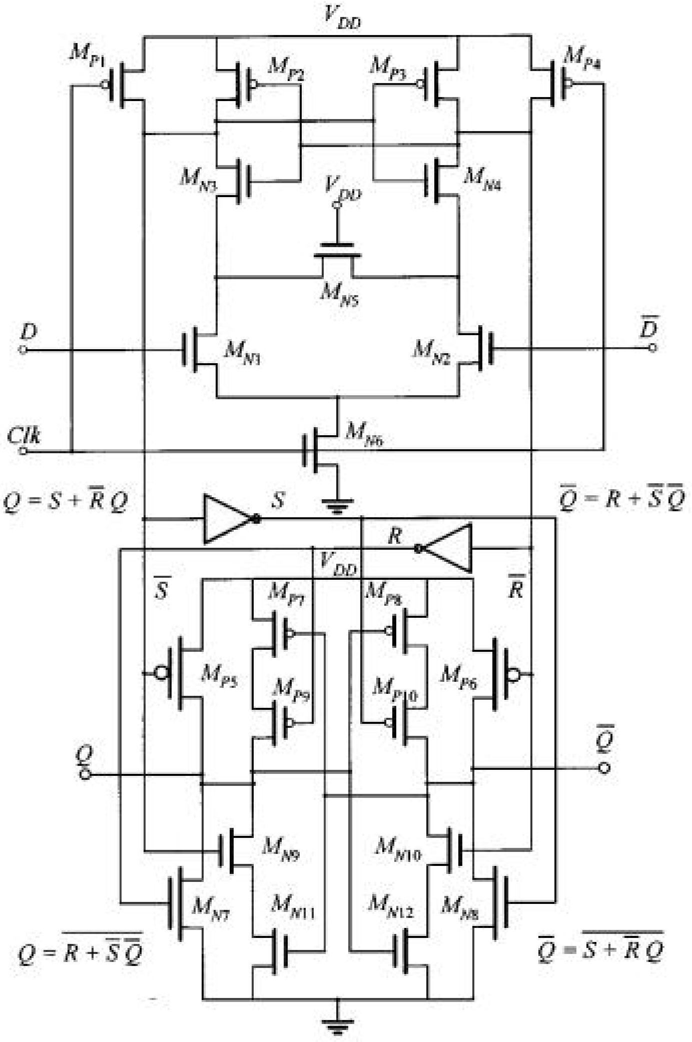
Title of the circuit : Improved Sense-Amplifier-Based Flip-Flop

Theory/Description : The modified sense-amplifier-based flip-flop (SAFF) improves the conventional SAFF by redesigning the slave latch stage. It uses a symmetric latch topology that reduces delay and balances the true and complementary output paths. This modification removes the main speed bottleneck of the traditional SR latch, improving clock-to-output performance. The new structure also enhances driving capability and reduces power and crowbar current. Overall, the modified SAFF achieves higher speed and better signal symmetry, making it suitable for high-performance digital circuits.

Reason to reproduce with eSim : Reproducing the modified SAFF in eSim/PSPICE helps validate the circuit's theoretical design by analyzing its timing behavior, speed, and output characteristics under realistic CMOS models. Simulation allows us to observe how the modified symmetric latch improves delay and signal balance compared to the conventional SAFF. It also helps evaluate power and performance trade-offs before hardware implementation, ensuring the design is efficient and reliable.

Expected Outcome: The modified SAFF captures the input data at the clock edge and stores it at the output Q with high speed and stability. It produces Q and $\overline{Q}$ signals with nearly equal delay due to its symmetric latch design, reducing the timing imbalance seen in conventional SAFFs. The improved structure results in faster output transitions and better driving capability, making the flip-flop more reliable and suitable for high-performance digital circuits.

Circuit Diagram:



Research Paper/Journal/etc. :

Improved Sense-Amplifier-Based Flip-Flop: Design and Measurements Borivoje Nikolic´, Member, IEEE, Vojin G. Oklobdzija ˇ , Fellow, IEEE, Vladimir Stojanovic´, Wenyan Jia, Member, IEEE, James Kar-Shing Chiu, and Michael Ming-Tak Leung