Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and Implementation of an 8×1 Multiplexer Using 2×1 Multiplexer Modules

Theory/Description :

An 8×1 multiplexer is a combinational circuit that selects one of eight input signals and routes it to a single output based on three select lines. In this design, the 8×1 MUX is constructed using 2×1 multiplexers arranged in a hierarchical manner. The select lines control each stage of the circuit, gradually reducing the number of inputs until the final output is obtained. This modular approach ensures efficient hardware utilization, reduced propagation delay, and simplified design, making the circuit suitable for high-speed digital systems, embedded applications, and VLSI implementations.

Reason to reproduce with eSim :

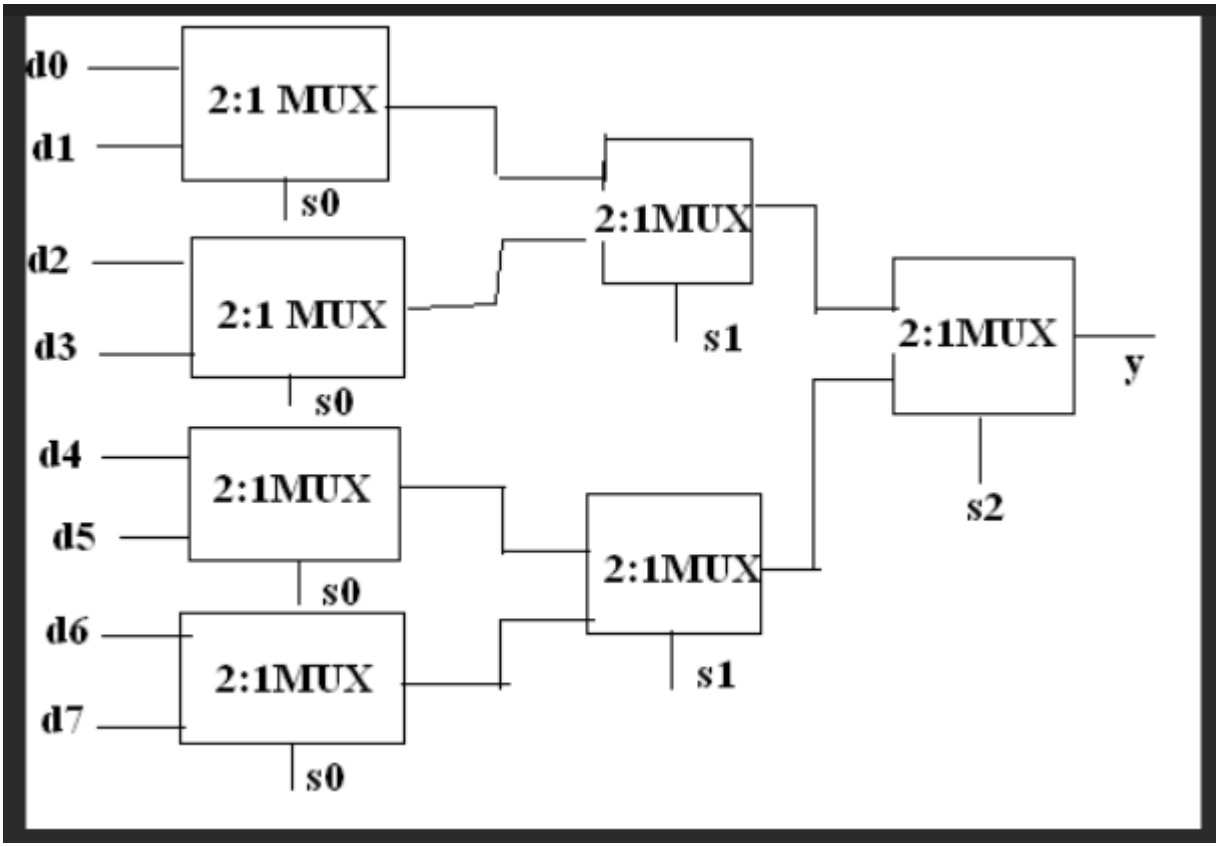
This circuit is well suited for reproduction using eSim because it is an open-source, SPICE-based simulation tool that enables accurate modeling and verification of digital circuits. eSim provides an interactive and user-friendly environment to design, simulate, and analyze the behavior of multiplexers, allowing easy verification of select logic and output correctness. The hierarchical design using 2×1 MUX building blocks makes the circuit ideal for educational purposes, as each stage can be tested independently. Additionally, eSim supports waveform analysis, logical validation, and design optimization, helping to identify delays and improve efficiency, making it an effective platform for learning, experimentation, and circuit validation.

Expected Outcome/outputs :

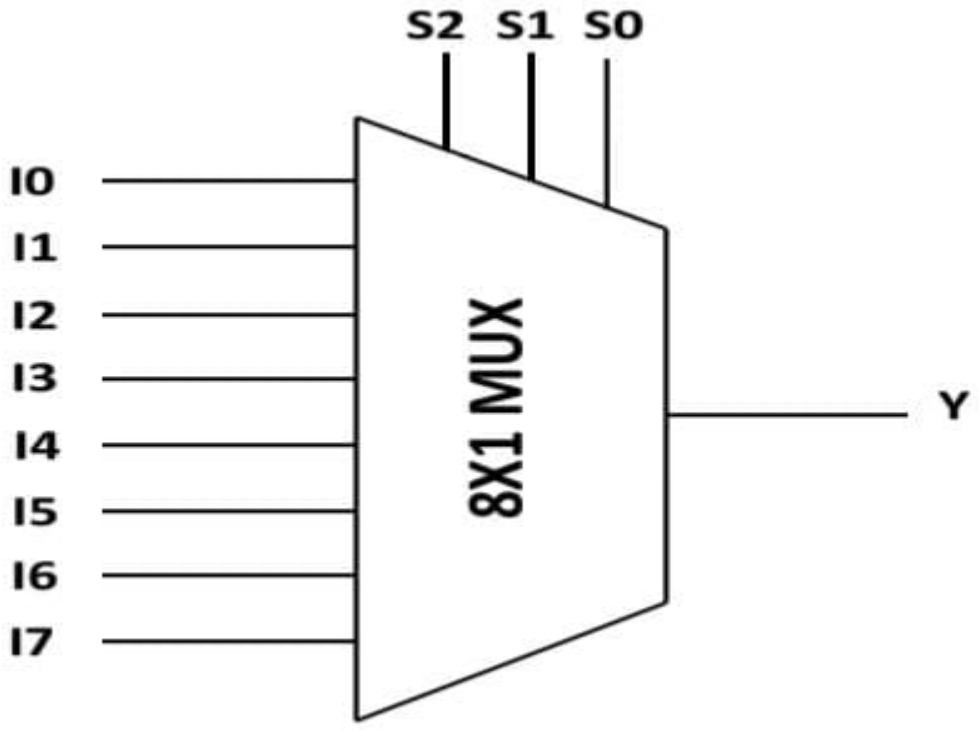
When the 8×1 multiplexer circuit is simulated or implemented, the output is expected to correctly reflect the value of the selected input line based on the combination of the three select signals. For every valid select input, only one of the eight data inputs will be routed to the output while all others remain inactive. The correctness of the circuit can be validated by observing the output waveforms in simulation and comparing them with the expected truth table. Stable output transitions, minimal propagation delay, and proper switching

behavior confirm the accurate functioning and efficiency of the multiplexer design.

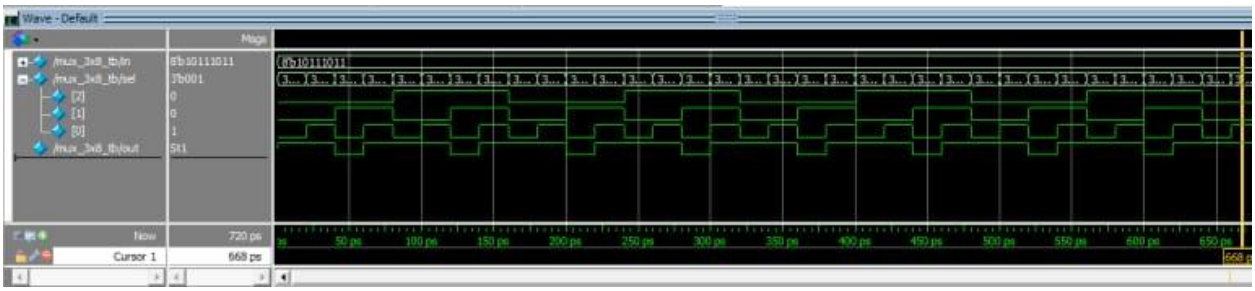
Circuit Diagram(s) :



Block Diagram (s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :



Enable	Select Inputs			Output
E	S2	S1	S0	Y
0	X	X	X	0
1	0	0	0	I_o
1	0	0	1	I_1
1	0	1	0	I_2
1	0	1	1	I_3
1	1	0	0	I_4
1	1	0	1	I_5
1	1	1	0	I_6
1	1	1	1	I_7

Research Paper/Journal/etc. :

Title : Designing an 8x1 Multiplexer Using 2x1 Multiplexers in Verilog
Author : Mahnoor Zia
Page No. : Nil
Link : Designing an 8x1 Multiplexer Using 2x1 Multiplexers in Verilog | by Mahnoor Zia | Medium

Source/Reference(s) :

1. **https://youtu.be/uoBZZ53Okvo?si=cHKWML2Soo8KmG65**
2. **Designing an 8x1 Multiplexer Using 2x1 Multiplexers in Verilog | by Mahnoor Zia | Medium**
3. **Design and implement the 8x1 MULTIPLEXER with 2x1 MULTIPLEXERs program using Verilog HDL - IC Applications and ECAD Lab | vikramlearning.com**

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.