Circuit Simulation Project

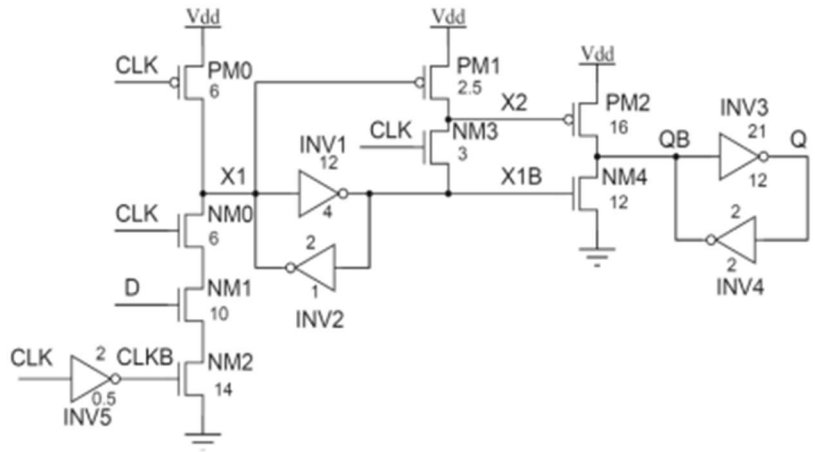
https://esbn.fossee.tn/ctrcuit-simutatton-project

Name of the participant: S.Pandigarajan

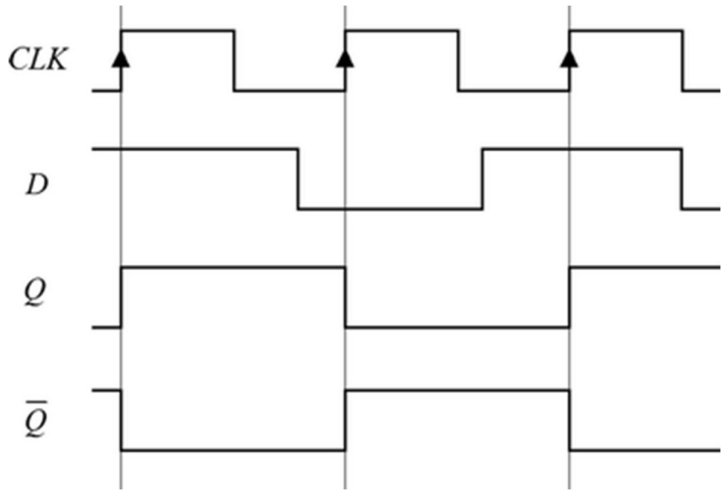
Title of the circuit: Dual Dynamic Node Hybrid Flip Flop using Esim

Theory/Deccription: The Dual Dynamic Node Hybrid Flip-Flop (DDFF) employs a pseudo-dynamic node (X1) and a dynamic node (X2), each supported by weak keeper inverters to enhance data retention and robustness. Unlike conventional designs such as the XCFF, the DDFF utilizes an unconditional shutoff mechanism at the input stage, simplifying control and improving operational reliability. The flip-flop operates in two phases: evaluation and precharge. During the evaluation phase (CLK = 1), data evaluation and conditional latching occur based on the overlap of the clock and its complement. When the input is asserted during this overlap, the internal node X1 discharges, triggering a state transition that propagates to the output while maintaining stability for the remainder of the evaluation period. In the precharge phase (CLK = 0), node X1 is restored, and node X2 dynamically retains its charge, preserving the output state. This dual-node dynamic operation enables efficient latching behavior with reduced power consumption and improved performance.

Circuit Diagram(s)



Results (Input, Output waveforms and/or Multimeter readings):



Source/Reference(s):

Titte of the Paper: Performance Evaluation of Pulse Triggered Flip flops in 32 nm COWS Regime

Name of the journal/Publication: IEEE Solid State Circuits Author(s): K. Absel, L. Manuel, and R. K. Kavitha

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Link: https://ieeexplore.ieee.org/document/10141264