Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay, that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open-source resource database.

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Title of the circuit: Enhanced SEPIC DC–DC Converter with Simple Analog Voltage Feedback Using eSim

Theory/Description : Single-Ended Primary Inductor Converter (SEPIC) is a DC–DC power converter capable of producing an output voltage that can be either higher or lower than the input voltage while maintaining the same output polarity. It is widely used in power management applications where the input voltage varies over a wide range.

The basic SEPIC converter consists of two inductors, a series coupling capacitor, a controlled switching device, a diode, and an output capacitor. When the switch is turned ON, energy is stored in the inductors. When the switch is turned OFF, the stored energy is transferred to the output through the diode, charging the output capacitor.

In this work, the basic SEPIC circuit is enhanced by adding a simple analog feedback network using a resistor divider, a Zener diode, and an NPN transistor. The feedback circuit senses the output voltage and automatically limits excessive output voltage by reducing the base drive of the switching transistor. This improves voltage regulation without using complex PWM controller ICs.

Reason to reproduce with eSim : eSim is an open-source EDA tool, making the design accessible to students and researchers.

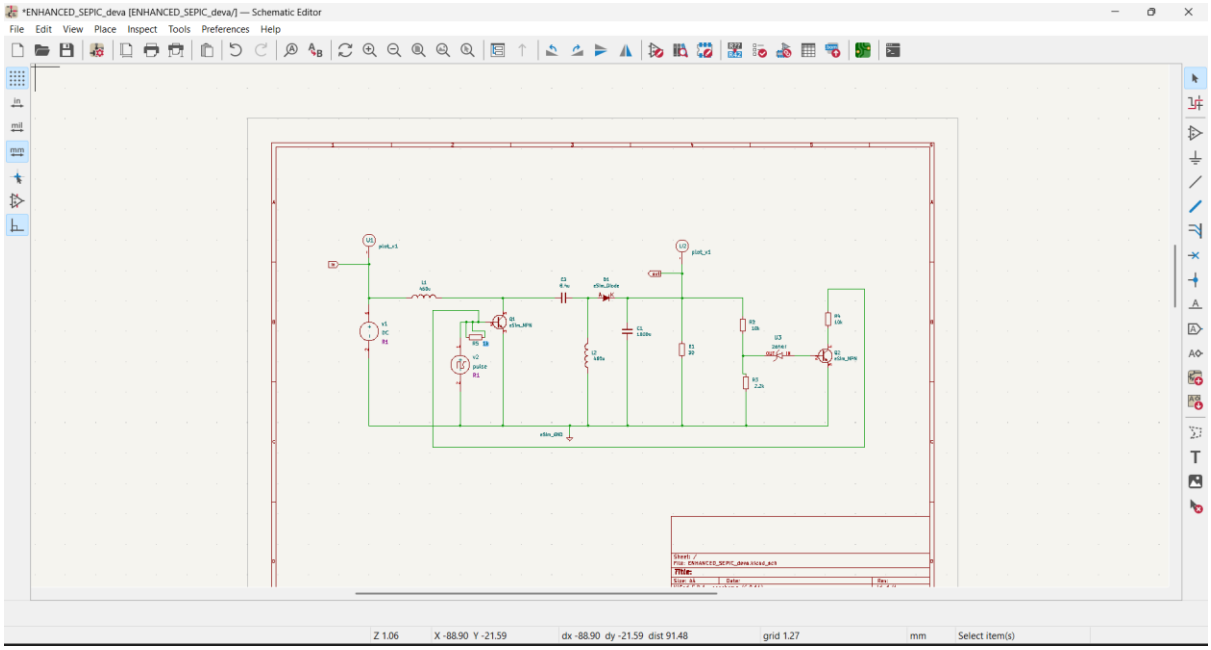
Simulation in eSim allows verification of voltage regulation behavior and feedback effectiveness.

Expected Outcome/outputs : When simulated in eSim:

- **The output voltage initially increases as the converter starts.**

- **Once the output reaches the Zener-set threshold, the feedback transistor turns ON.**
- **The feedback reduces the base current of the switching transistor.**
- **The output voltage stabilizes around the desired level instead of continuously increasing.**
- **The output voltage waveform shows controlled rise and regulation.**

Circuit Diagram(s) :



Block Diagram::

DC Input

|

v

SEPIC Power Stage (L1, L2, C, Switch, Diode)

|

v

Output Filter & Load

|

v

Voltage Sensing (Resistor Divider)

|

v

Zener Reference

|

v

Feedback Transistor

|

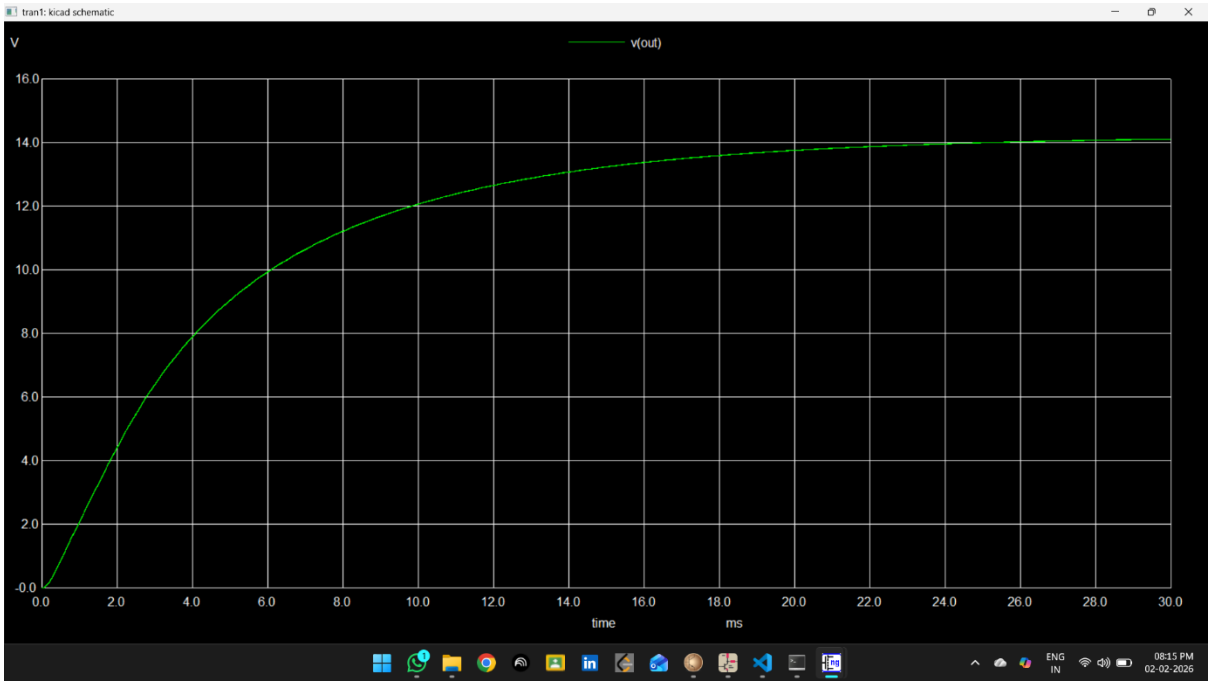
v

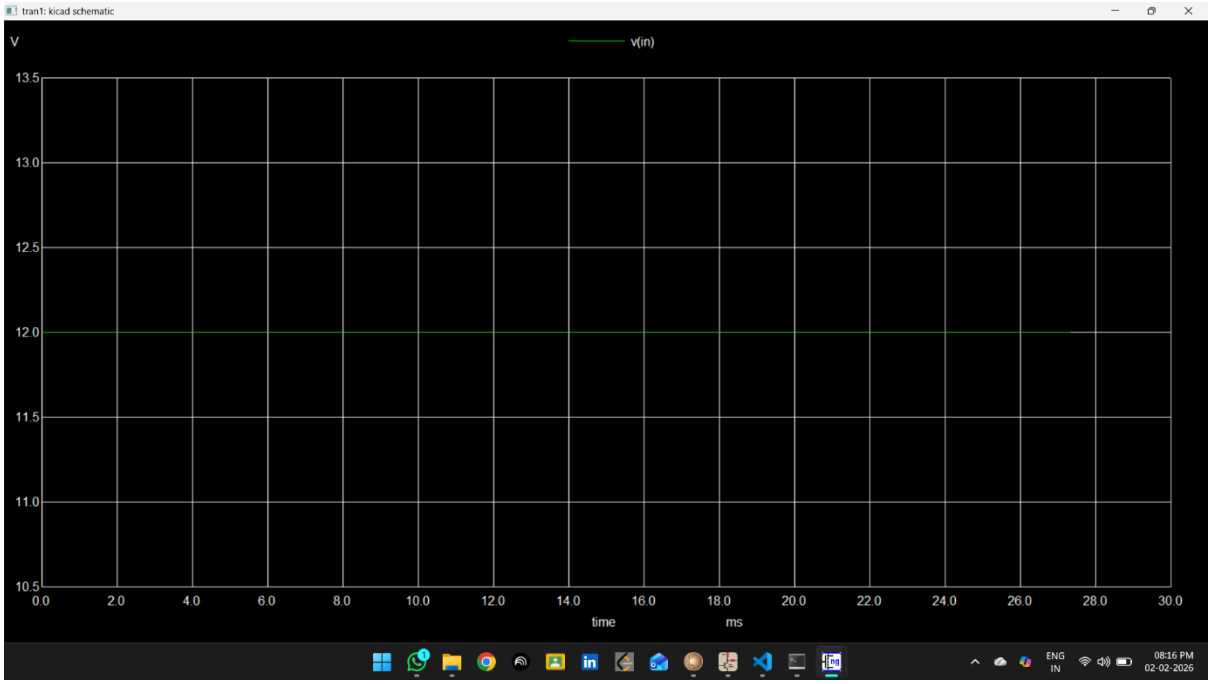
Switch Control (Base Current Limiting)

Expected Results (Input, Output waveforms and/or Multimeter readings) :

Vin:12V

Vout: after 14V the graph is getting a constant and stable voltage this is due to the feedback npn transtor and the controller Zener diode





Research Paper/Journal/etc. : Title:
Analysis and Design of SEPIC Converter for DC–DC Power Conversion

Author:
R. Erickson, D. Maksimović

Page No.:
Relevant chapters on SEPIC topology

Link:
https://www.sciencedirect.com/topics/engineering/sepic-converter
or
https://scholar.google.com (search: *SEPIC converter analysis*)

Wurth Elektronik -
https://www.weonline.com/en/components/applicationguide/sepic_converter

Texas Instrumentation - https://www.ti.com/lit/an/slyt309/slyt309.pdf

Muhammad H.Rashid, PhD - Power Electronics Handbook, chapter 13, chapter 14
