Name of the participant:

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Title of the circuit:

Fine-Grained Clock-Gated 4-Bit Counter for Low-Power Digital Systems

Theory / Description:

Clock gating is an effective low-power design technique used to reduce dynamic power consumption by disabling the clock to inactive circuit blocks. In conventional synchronous counters, all flip-flops receive the clock irrespective of switching activity, resulting in unnecessary power dissipation. This circuit implements a **latch-based fine-grained clock gating architecture**, where enable conditions are captured using level-sensitive latches during the low phase of the clock. The latched enable signals are ANDed with the global clock to generate **glitch-free gated clocks** for individual counter bits, allowing only the required flip-flops to toggle.

Reason to reproduce with eSim:

The proposed circuit is well suited for reproduction using **eSim**, as it demonstrates a widely used **industry-standard low-power clock gating technique** in an open-source simulation environment. Migrating this design to eSim enables verification of latch-based glitch-free clock gating without proprietary tools, supports educational learning in low-power VLSI design, and contributes to an open repository of power-efficient digital circuits.

Expected Outcome / Outputs:

Upon simulation, the counter increments correctly when the enable signal is active, while unused flip-flops remain clock-gated. Individual gated clocks toggle only when required, demonstrating reduced switching activity. The output carry is asserted when all counter bits reach logic high under enable condition, validating correct fine-grained operation.

Circuit Diagram(s):

A complete gate-level schematic consisting of:

- Level-sensitive latches
- AND-based clock gating logic
- D flip-flops
- Inverter for clock phase generation
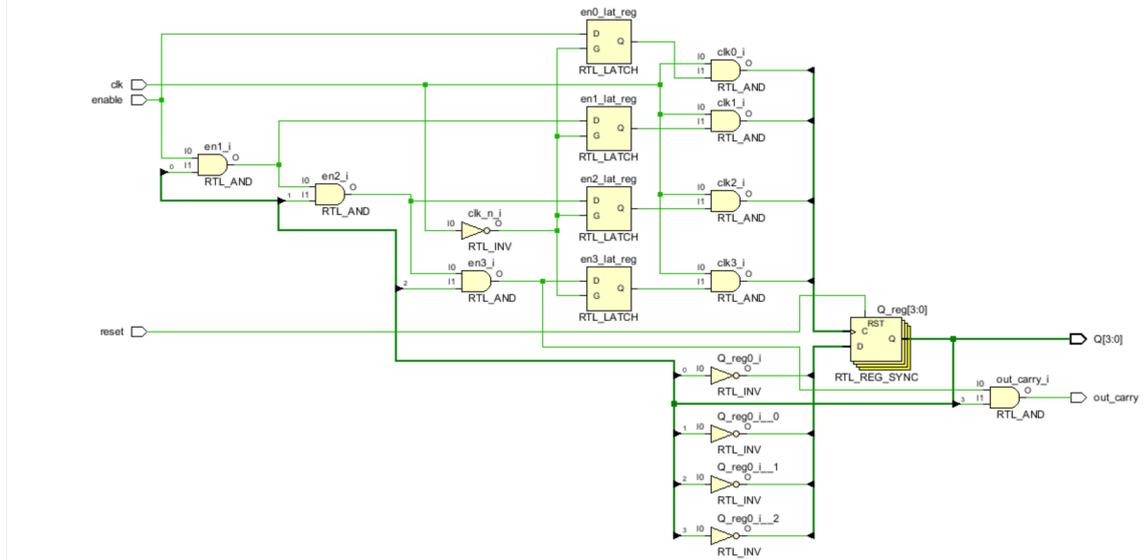
Expected Results (Input, Output waveforms / Multimeter readings):

- Global clock waveform with continuous toggling
- Gated clock waveforms showing suppressed clock pulses when enable is inactive
- Counter outputs (Q0–Q3) incrementing correctly
- Output carry asserted when Q0–Q3 are logic high
- Reduced clock switching activity observed for higher-order bits.

Research Paper / Journal / etc.:

Title:
Glitch-Free Clock Gating Techniques for Low-Power Synchronous Circuits

Author:
J. M. Rabaey, A. Chandrakasan, B. Nikolic

Page No.:
Relevant sections on clock gating and low-power sequential logic

Link:
https://ieeexplore.ieee.org/document/1207037
(or Google Scholar equivalent)

Source / Reference(s):

- J. M. Rabaey et al., *Digital Integrated Circuits: A Design Perspective*, Prentice Hall
- IEEE papers on latch-based clock gating techniques