Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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Title of the circuit : Design and Simulation of a Clock-Gating Cell for Low-Power VLSI Systems using eSim

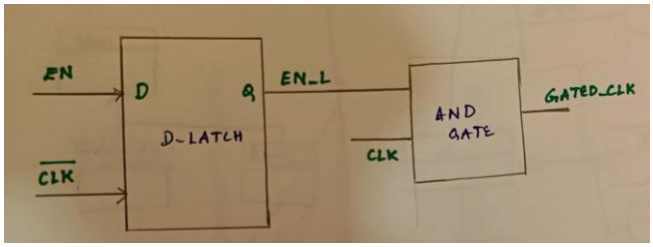
Description : Clock gating is an effective low-power technique used in VLSI systems to reduce dynamic power consumption by preventing unnecessary clock switching in idle circuit blocks. Since the clock signal has the highest switching activity, continuous toggling leads to significant power dissipation. A clock-gating cell operates by controlling the clock signal using an enable condition while ensuring glitch-free operation. This is achieved by sampling the enable signal through a level-sensitive latch when the clock is inactive and then combining the latched enable with the clock using a logic gate to generate a gated clock output. When enabled, the clock propagates normally, and when disabled, clock transitions are blocked, thereby reducing switching activity. In this work, a CMOS-based clock-gating cell is designed and simulated using eSim to demonstrate its functionality and suitability for low-power VLSI applications.

Reason to reproduce with eSim : The clock-gating cell is well suited for reproduction using eSim as it is a fundamental CMOS-based VLSI building block that can be accurately modeled and simulated at the transistor and logic levels. eSim provides an open-source platform with integrated schematic capture and simulation capabilities, making it ideal for verifying the functional correctness and timing behavior of clock-gating circuits. Reproducing this circuit in eSim has strong educational value, as it allows visualization of glitch-free clock control and power-saving concepts in synchronous digital systems. Additionally, implementing the clock-gating cell in eSim helps extend the availability of low-power VLSI design examples in an open-source environment.

Expected Outcome/outputs : Upon simulation, the clock-gating cell is expected to produce a gated clock output that correctly follows or blocks the input clock based on the enable signal. When the enable signal is asserted, the gated clock should toggle synchronously with the input clock, allowing normal operation of downstream circuits. When the enable signal is deasserted, the gated clock transitions should be suppressed, demonstrating effective clock disabling. The correctness of the circuit can be validated by observing glitch-free gated clock

waveforms in transient simulations and verifying proper enable-controlled behavior, which confirms the functional operation of the clock-gating cell.

Circuit Diagram(s) :



Signal	Description
CLK	Input clock signal (pulse source)
$CL\bar{K}$	Inverted clock (generated using inverter)
EN	Enable control signal
EN_L	Latched enable output
GATED_CLK	Output gated clock

Component	Purpose	Value / Type
Voltage Source	VDD	1.8 V
Ground	GND	0 V
Pulse Voltage Source	Clock (CLK)	PULSE(0, 1.8 V, 0, 1 ns, 1 ns, 10 ns, 20 ns)
DC / Pulse Source	Enable (EN)	0 V / 1.8 V
Inverter	Generate $CL\bar{K}$	CMOS inverter
D-Latch	Latch enable safely	Level-sensitive
AND Gate	Clock gating	2-input AND

Behaviour Table:

EN	CLK	GATED_CLK
0	0 / 1	0
1	0 / 1	CLK

Expected Results (Input, Output waveforms and/or Multimeter readings) : During simulation, the input clock (CLK) is expected to appear as a periodic square waveform, while the enable signal (EN) switches between logic LOW (0 V) and logic HIGH (1.8 V). When EN is HIGH, the gated clock output (GATED_CLK) should follow the input clock waveform. When EN is LOW, the gated clock output should remain at logic LOW, indicating successful clock blocking. The latched enable signal (EN_L) is expected to update only when the clock is LOW, ensuring glitch-free operation. The correct functionality will be verified by observing the input and output waveforms in transient simulation.

Research Paper/Journal/etc. :

Title: Glitch-Free Clock Gating: A Survey and Design Methodology

Author(s): S. Raje, M. Sarrafzadeh

Link: https://ieeexplore.ieee.org/document/7124828
