Research Migration Project

https://esim.fossee.in/research-migration-project

The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant : DINESH T

Affiliation / Institution : ANNA UNIVERSITY/CHENNAI INSTITUTE OF TECHNOLOGY

Title of the circuit : Implementation of Synchronous Serial-In Serial-Out (SISO) Shift Register Using D Flip-Flops in eSim Circuit Simulator

Theory/Description :

Shift registers are fundamental sequential digital circuits widely used for data storage, transfer, and synchronization in digital systems. A Serial-In Serial-Out (SISO) shift register accepts data serially, one bit per clock cycle, and outputs the data serially after a fixed delay determined by the number of storage elements used.

In this work, a synchronous SISO shift register is implemented using D flip-flops. The circuit is constructed by cascading multiple D flip-flops such that the Q output of each flip-flop is connected to the D input of the next flip-flop. All flip-flops are driven by a common clock signal, ensuring synchronous operation. On each rising edge of the clock, the input data bit is shifted through the chain of flip-flops. The serial output is obtained from the Q output of the final flip-flop. A reset signal is provided to initialize the register to a known state before operation

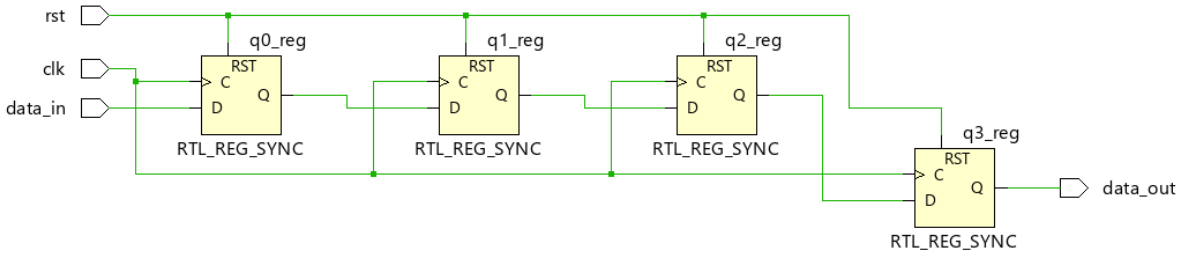
Reason to reproduce with eSim :

This circuit is suitable for reproduction using eSim because shift registers are widely used educational and research circuits that benefit from open-source simulation tools. Migrating this design to eSim eliminates dependency on proprietary software while ensuring transparency, reproducibility, and accessibility. The circuit serves as an excellent learning resource for understanding sequential logic, flip-flop behavior, and clocked digital systems. Additionally, eSim allows easy waveform analysis and validation of timing behavior, making it ideal for academic and research purposes.

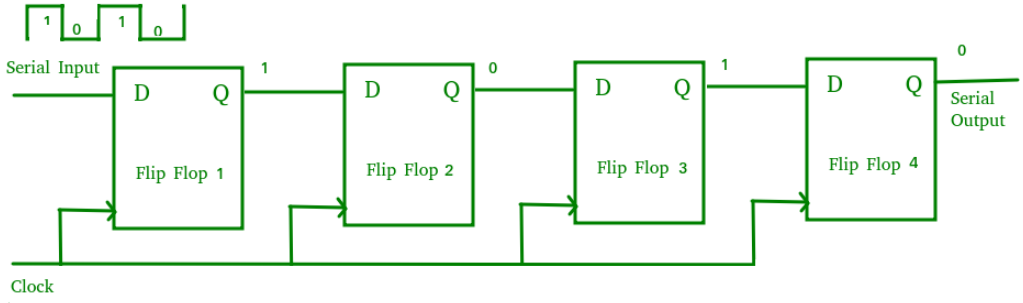
Expected Outcome/outputs :

When simulated, the circuit is expected to demonstrate correct serial shifting of data through the D flip-flops on each rising edge of the clock. The serial output should reproduce the input data after a delay equal to the number of flip-flops used. The reset operation should correctly clear all stored bits. The functionality can be validated through waveform observation of input, intermediate flip-flop outputs, and final output.

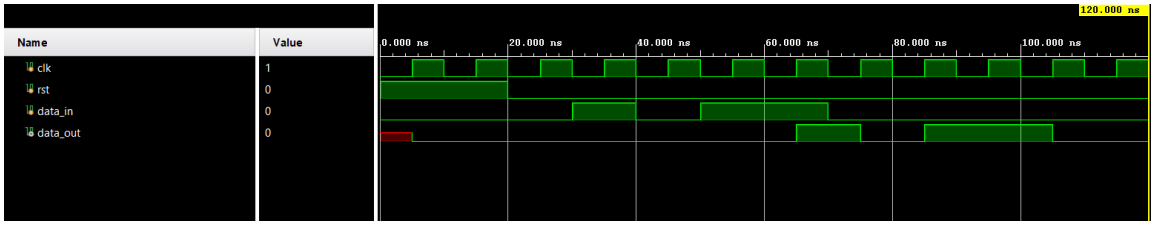
Circuit Diagram(s) :



Block Diagram (s) :



Expected Results (Input, Output waveforms and/or Multimeter readings) :



Research Paper/Journal/etc. :

Title : Design of Serial in Serial out and Serial in Parallel out Shift Register Using Double Edge Triggered D Flip Flop

Author : Namrata Rapartiwar, Vinod Kapse

Page No. :505-508

Link : https://www.ijetae.com/files/Volume4Issue7/IJETAE_0714_72.pdf

Source/Reference(s) :

1. **Rapartiwar, Namrata, and Vinod Kapse. *"Design of Serial in Serial out and Serial in Parallel out Shift Register Using Double Edge Triggered D Flip Flop."* International Journal of Emerging Technology and Advanced Engineering (IJETAE), Vol. 4, Issue 7, July 2014, pp. 505–508.**
2. **M. Morris Mano and Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th Edition, Pearson Education.**
3. **R. P. Jain, *Modern Digital Electronics*, 4th Edition, McGraw-Hill Education.**
4. **eSim Documentation, FOSSEE, IIT Bombay – https://esim.fossee.in**
