

Research Migration Project

<https://esim.fossee.in/research-migration-project>



The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

Name of the participant :

Suraj

Affiliation / Institution :

Department of Electrical and Electronics Engineering, Rajiv Gandhi Institute of Petroleum Technology (RGIPT), Jais, Amethi, Uttar Pradesh, India.

Title of the circuit :

Design and Simulation of a Voltage to Time Converter With ReLU Transfer Curve Using eSim.

Theory/Description :

A Voltage-to-Time Converter (VTC) with a built-in Rectified Linear Unit (ReLU) characteristic maps an analog input voltage to a time-domain pulse whose width indicates the signal level. When the input is below a certain threshold, no output pulse is produced; for higher voltages, the pulse width increases approximately linearly, reproducing ReLU behavior. This approach is attractive for analog neural-network hardware because it can reduce repeated voltage-to-digital conversions between processing stages.

The circuit uses switched-capacitor sampling, a transconductance stage, and MOSFET-based evaluation logic to start and stop the output pulse. By choosing appropriate capacitor ratios, the slope of the ReLU curve and the dynamic range can be adjusted, while clocked sampling and evaluation phases allow periodic operation. The complete schematic will be recreated in eSim, and transient simulations will be carried out to study the input–output transfer curve, pulse-width variation with input voltage, and the main performance trends of the design.

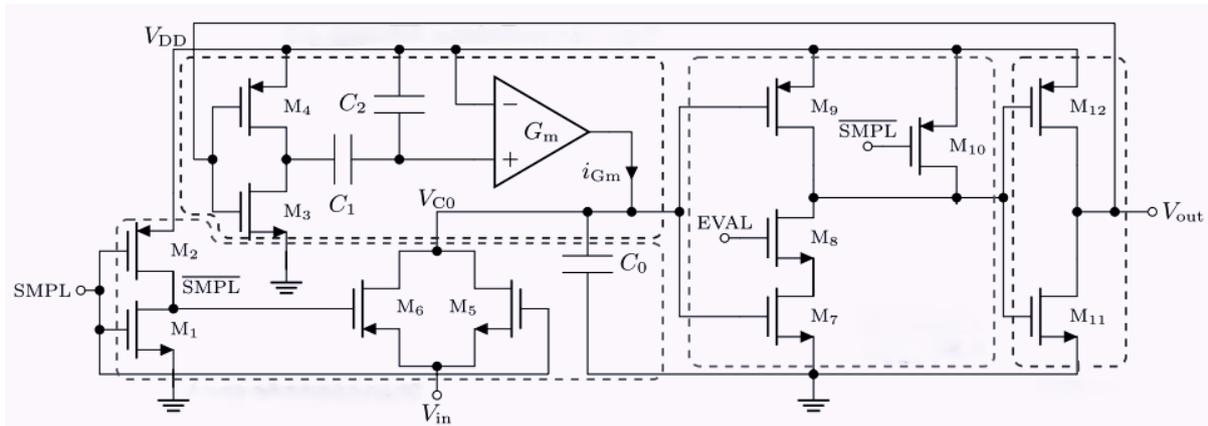
Reason to reproduce with eSim :

This circuit is suitable for migration to eSim because it is primarily based on schematic-level CMOS building blocks such as switches, capacitors, inverters, and transconductance stages that can be implemented using open-source SPICE models. Reproducing the design in eSim supports FOSSEE's objective of building an open-source repository of validated research circuits, enables educational use by students, and allows verification of published functionality without relying on proprietary simulation tools.

Expected Outcome/outputs :

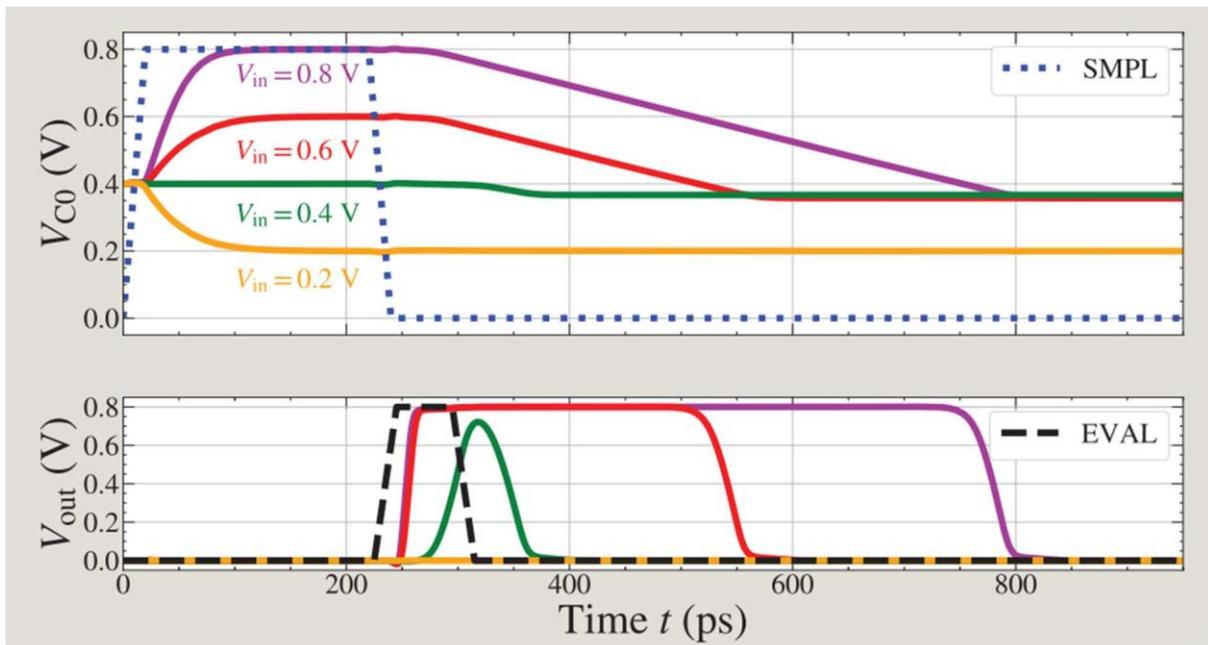
The migrated circuit is expected to demonstrate correct sampling and evaluation behavior for different input voltages. Transient analysis will verify pulse generation, pulse termination, and threshold-dependent operation corresponding to the ReLU characteristic.

Circuit Diagram(s) :



*refer the research paper 1 , figure 1.

Expected Results (Input, Output waveforms and/or Multimeter readings) :



*refer from the research paper(1), figure 2.

Research Paper/Journal/etc. :

- 1) Jakob Finkbeiner, "An Energy-Efficient Voltage-to-Time Converter With Built-in ReLU Activation Function in 22-nm FDSOI," *IEEE Solid-State Circuits Magazine*, Winter 2025. DOI: [10.1109/MSSC.2024.3490212](https://doi.org/10.1109/MSSC.2024.3490212).

Source/Reference(s) :

- 1) Design of Analog CMOS Integrated Circuits, Behzad Razavi, McGraw-Hill, 2nd Edition.
-

Note: Fields marked with an asterisk (*) are mandatory and must be filled for successful submission.