

# Research Migration Project

<https://esim.fossee.in/research-migration-project>



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The Research Migration Project is an initiative of FOSSEE, IIT Bombay that promotes the use of eSim for reproducing published research circuits originally implemented using proprietary simulation tools. The objective is to migrate these validated designs to eSim to build an open source resource database.

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## **Name of the participant :**

Shreyansh Daksha

## **Affiliation / Institution :**

Department of Electrical and Electronics Engineering,  
Rajiv Gandhi Institute of Petroleum Technology (RGPT),  
Jais, Amethi, Uttar Pradesh, India.

## **Title of the circuit :**

Design of a Current Mirror–Based Bandgap Voltage Reference

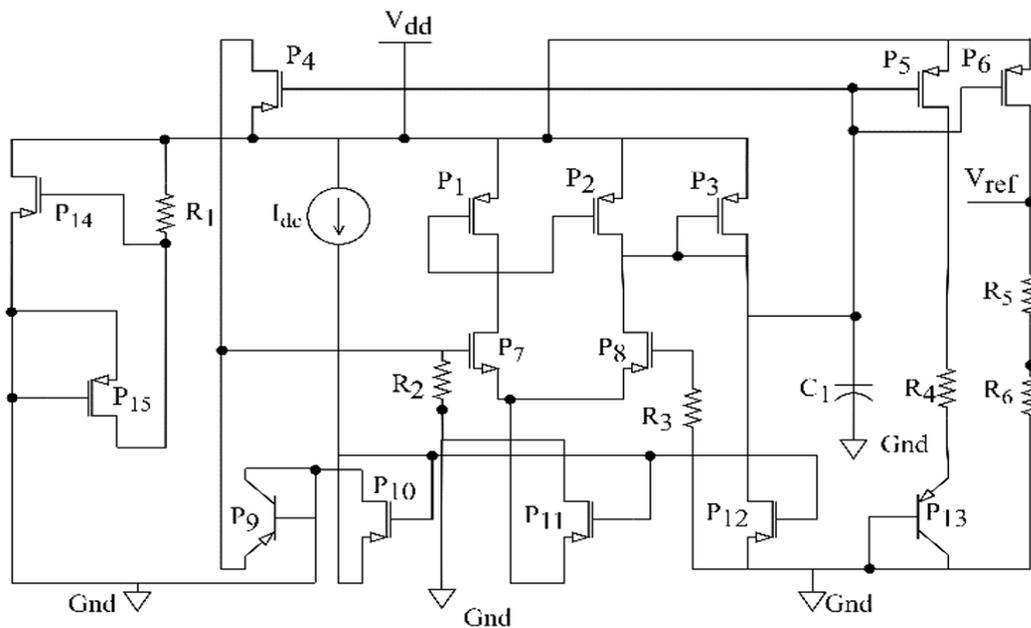
## **Theory/Description :**

A current mirror–based Bandgap Voltage Reference (BGR) is designed ( 90 nm CMOS technology) , a two-stage current mirror is used to ensure uniform current flow and improved bias stability. The circuit operates using a current-mode approach, which supports low voltage operation and enhances overall stability. The proposed BGR functions constantly over a temperature range of  $-40^{\circ}\text{C}$  to  $160^{\circ}\text{C}$ , exhibiting a stability of 0.7%. With a supply voltage of 1.4 V, the circuit generates a reference voltage of 1.262 V while consuming  $1.4\ \mu\text{A}$ , corresponding to a power consumption of  $1.6\ \mu\text{W}$ . These features make the design well suited for low-power CMOS applications.

## **Expected Outcome/outputs :**

When the supply is applied, the BGR smoothly starts up and the output voltage rises to about **1.26 V**. After a short initial transient, the voltage settles quickly and remains stable without any noticeable overshoot or oscillations. This shows that the circuit has a reliable startup and maintains a steady reference voltage over time.

## **Circuit Diagram(s) :**



**Expected Results (Input, Output waveforms and/or Multimeter readings) :**

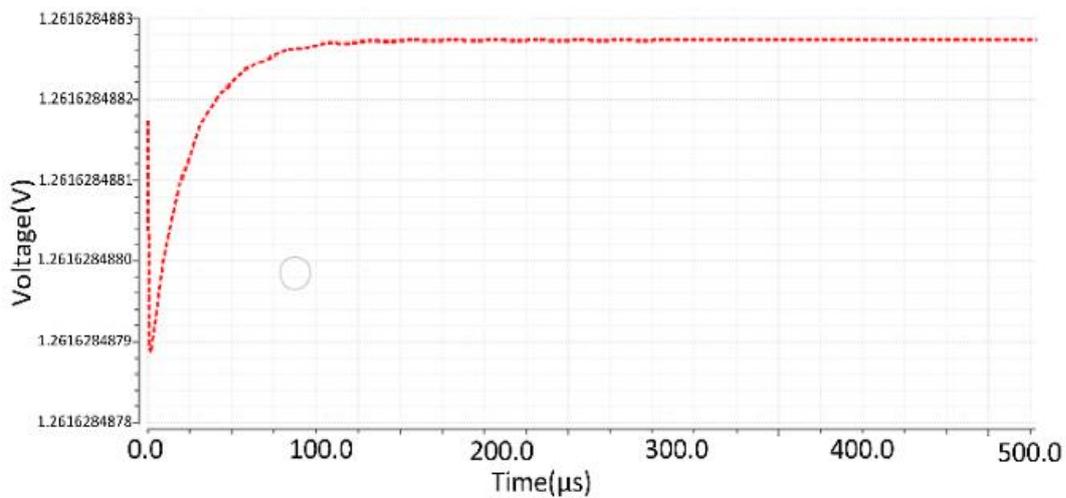


Fig. 7. Transient analysis of the proposed BGR circuit.

\*present in the research paper 1, figure7

**Research Paper/Journal/etc. :**

1) Joy, Upal Barua, Arindom Chakraborty, Jyoti Kandpal, and Md Shahbaz Hussain. "Design of a Bandgap Voltage Reference Circuit in 90 nm CMOS Process." In 2024 15th International Conference on Computing Communication and Networking Technologies (ICCCNT), pp. 1-5. IEEE, 2024.

<https://doi.org/10.1109/icccnt61001.2024.10724041>

**Source/Reference(s) :**

1) Razavi, Behzad. Design of analog CMOS integrated circuits. 2005.

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**Note:** Fields marked with an asterisk (\*) are mandatory and must be filled for successful submission.