Analysis of Low-Power Dynamic Comparator Architectures
(PROJECT PROPOSAL SYNOPSIS)

Introduction

Dynamic comparators are essential components in modern low-power mixed-signal systems, particularly in analog-to-digital converters (ADCs), data converters, and sensor interfaces. Their clocked operation allows them to consume power only during active comparison, making them well-suited for energy-constrained applications. However, as CMOS technology scales down and supply voltages reduce, achieving low power consumption while maintaining high-speed and reliable decision-making becomes increasingly challenging.

To address these challenges, recent research has focused on transistor-level optimization and architectural enhancements in dynamic comparator designs. Instead of relying on behavioral models, research-level designs emphasize regenerative latching behavior, controlled current paths, and multi-stage operation to reduce dynamic power dissipation and improve performance. This project focuses on migrating such research-oriented comparator circuits into the eSim simulation environment to study their behavior at the circuit level.

Reference Paper Information

- **Title:** *Analysis of Low Power Dynamic Comparator*

- **Authors:** M. Sai Navya, U. Koti Reddy, N. Yaswanth Kumar, G. Sai Krishna, P. Lakshman

- **Journal Name:** *International Journal of Innovative Technology and Exploring Engineering (IJITEE)*

- **Publisher:** Blue Eyes Intelligence Engineering and Sciences Publication

- **Volume:** 9, Issue**:** 7

- **Month and Year of Publication:** May 2020

- **ISSN:** 2278-3075

- **Technology Node Used:** 130 nm CMOS technology

- **Key Contribution:**

    - Comparative analysis of conventional and proposed dynamic comparator architectures.
    - Introduction of cascade dynamic comparator and two-stage comparator with cross-coupled latch.

- Demonstration of reduced dynamic power through transistor sizing optimization, particularly for cascade transistors.

Proposed eSim Implementation

The objective of this work is not to replicate exact 130 nm fabrication results, as eSim uses generic MOSFET models, but to faithfully migrate the circuit architectures and verify qualitative performance trends reported in the paper. Four comparator architectures will be implemented and simulated under identical conditions in eSim:

1. **Conventional Dynamic Comparator**
   This circuit serves as the baseline design. It consists of a differential input pair, a clock-controlled tail transistor, and precharge transistors at the output nodes. Transient simulations will be performed to observe precharge and evaluation behavior, output discharge characteristics, and dynamic power consumption.
2. **Proposed Cascade Dynamic Comparator**
   In this architecture, additional cascade transistors are inserted in the evaluation path to limit unnecessary current flow. These transistors reduce short-circuit current during evaluation. The widths of the cascade transistors will be varied to observe their effect on dynamic power consumption, replicating the optimization approach described in the paper.
3. **Conventional Dynamic Comparator with Cross-Coupled Latch**
   To improve output swing and regeneration speed, a cross-coupled latch is added as a second stage. The latch amplifies small voltage differences from the first stage into full-swing digital outputs. Transient response, decision time, and power consumption will be analyzed.
4. **Cascade Dynamic Comparator with Cross-Coupled Latch**
   This final architecture combines cascade current-limiting with strong positive feedback from a latch stage. It is expected to exhibit the lowest power dissipation and fastest decision time among all designs.

Expected Outcome

Through comparative transient simulations, this project will demonstrate how architectural evolution and transistor-level optimization reduce dynamic power consumption while improving speed and robustness. Although absolute numerical results may differ from the paper due to model limitations, the relative performance trends are expected to match the research conclusions.

Submitted by: NAGENDRA KUDVA, nagendrakudva21@gmail.com, B.tech ECE,
Manipal Institute of Technology, Manipal