Research Migration Project

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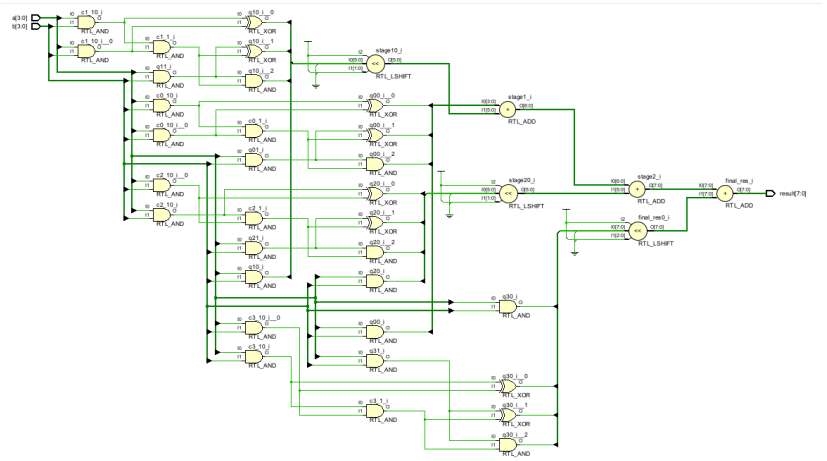
Title of the circuit : Design and Simulation of a 4x4 High-Speed Vedic Multiplier using Urdhva-Tiryakbhyam Sutra

1. Introduction Multipliers are critical components in Digital Signal Processing (DSP) and Arithmetic Logic Units (ALUs). Conventional multipliers like the Array Multiplier or Booth Multiplier suffer from high propagation delays due to sequential carry generation. This project implements a 4x4 Vedic Multiplier based on the ancient Indian mathematical sutra, "Urdhva-Tiryakbhyam" (Vertically and Crosswise). This algorithm allows for the simultaneous generation of partial products, making it significantly faster and more power-efficient than standard designs.

2. Working Principle The 4x4 Vedic Multiplier operates on the Urdhva-Tiryakbhyam sutra, which enables high-speed multiplication through parallel partial product generation. By decomposing 4-bit inputs into four 2-bit segments, the design processes vertical and crosswise products simultaneously using independent 2x2 logic blocks. These partial results are then aligned according to their binary weights via logical shifts (<<2 and <<4) and combined through a hierarchical summation stage. This structural hierarchy, implemented through modular Verilog logic, significantly reduces the critical path by eliminating the long carry-propagation delays found in traditional shift-and-add multipliers. Consequently, the design provides a stable and efficient 8-bit output, making it ideal for high-performance digital signal processing.



3. Conclusion The implemented Vedic Multiplier successfully demonstrates the efficiency of the Urdhva-Tiryakbhyam algorithm. By integrating Verilog HDL with eSim's spice environment, the project provides a robust framework for high-speed arithmetic circuit design. This design is highly suitable for low-power VLSI applications and real-time signal processing.

4. References

M. Durga Madhuri et al., "Implementation of High Speed Vedic Multiplier," *International Journal of Innovative Science and Research Technology*, Vol. 2, Issue 3, March 2017.