Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant :Yamini Menda

Title of the circuit :Design and implementation of 2-Bit Magnitude Comparator using GDI Technique

Theory/Description : In recent years, low power design has become one of the prime focuses for the digital VLSI circuit. Keeping the same in mind a new design of 2-Bit GDI based Magnitude Comparator has been proposed and implemented with the help of full adder which is the basic building block of ALU. Proposed GDI technique based magnitude comparator has an advantage of less power consumption with respect to various design parameters; less on-chip area covered as less number of transistors are required in circuit design as compared to conventional CMOS magnitude comparator. The circuit designed and simulated using eSim EDA Tool.

NOTE:-This project uses GDI Technique while it is entirely different from one of the previously proposed eSim project on Design of magnitude comparator

Circuit Diagram(s) :

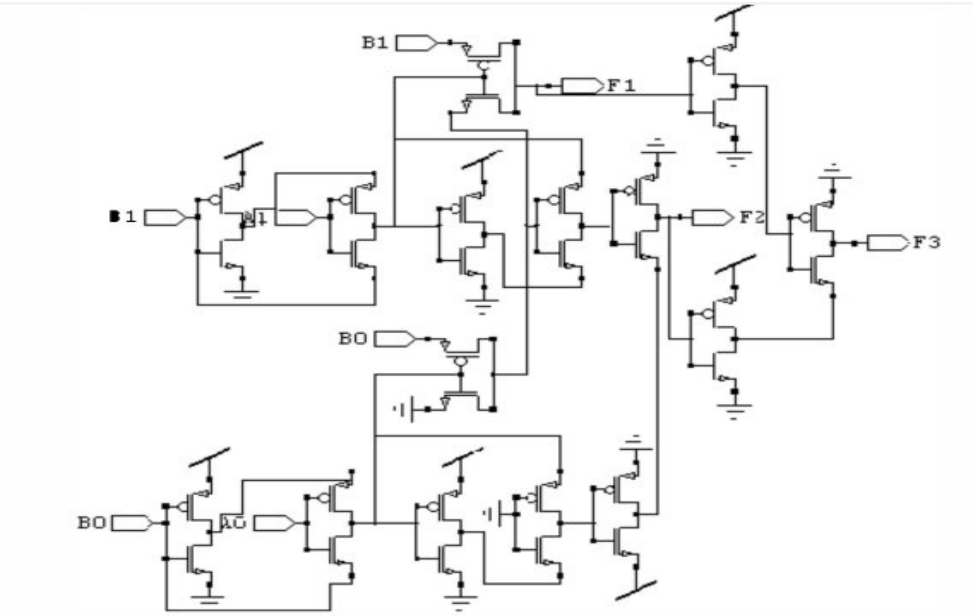

Fig. 6. Schematic of 2 Bit Magnitude Comparator using GDI Technique

Results (Input, Output waveforms and/or Multimeter readings) :

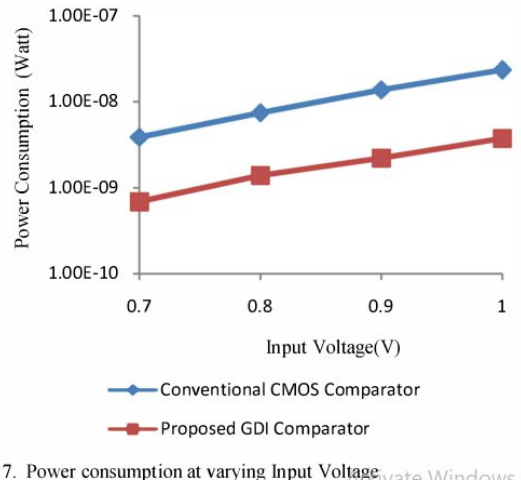

Fig. 7. Power consumption at varying Input Voltage

TABLE I. TRUTH TABLE OF 2 -BIT MAGNITUDE COMPARATOR

A1	A0	B1	B0	F2	F1	F3
0	0	0	0	1	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

Source/Reference(s) :https://ieeexplore.ieee.org/document/6909270

[1] V. Shekhawat, T. Sharma and K. G. Sharma, "2-Bit magnitude comparator using GDI technique," International Conference on Recent Advances and Innovations in Engineering (ICRAIE-2014), Jaipur, India, 2014, pp. 1-5, doi: 10.1109/ICRAIE.2014.6909270. keywords: {CMOS integrated circuits;Logic gates;CMOS technology;Inverters;MOS devices;Marine animals;Nanoscale devices;Magnitude Comparator;GDI Technique;Full Adder and Low Power},