CIRCUIT SIMULATION PROJECT

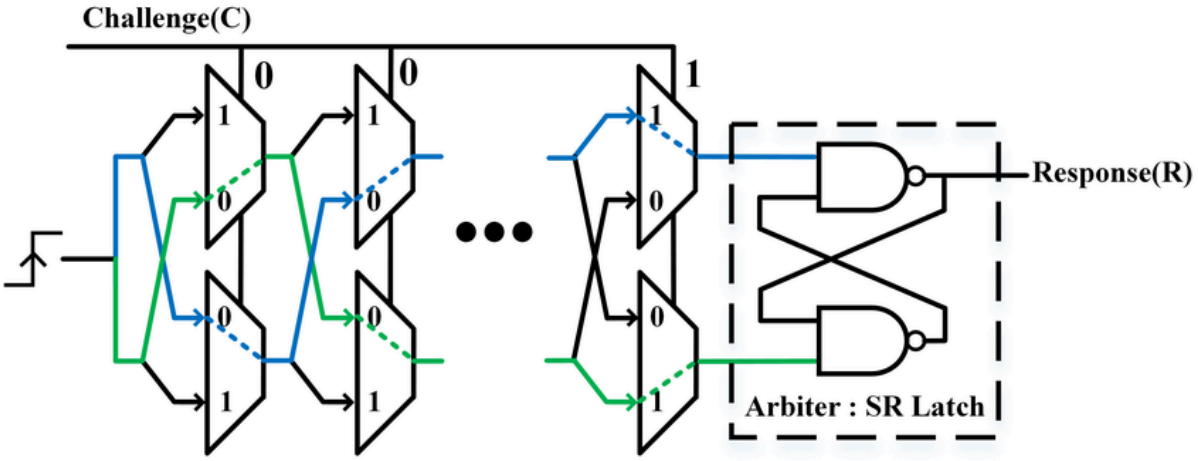
Name of the participant : JEYAPRANOV R.

Title of the circuit : Low-Power Silicon Fingerprinting: Design of a Symmetric 16-Stage Double-Data Arbiter PUF for IoT Security in 180nm Analog VLSI

Problem statement :

The rapid proliferation of IoT devices has intensified the need for low-cost, low-power hardware security primitives. Traditional cryptographic storage is vulnerable to physical attacks and requires non-volatile memory, which increases fabrication costs. While Arbiter Physically Unclonable Functions (APUFs) offer a promising solution for silicon fingerprinting, standard architectures suffer from systematic bias due to asymmetric routing and manufacturing gradients. This bias reduces the uniqueness and reliability of the generated keys, making them predictable. There is a critical need for a Double Data (DDQ) symmetric architecture that cancels these biases while being designed and verified within an Open-Source EDA (eSim) ecosystem to ensure accessibility and reproducibility in the semiconductor industry.

Circuit Diagram :



Primary Reference :

Y. Wang, G. Zhang, X. Mei, and C. Gu, "A High-Reliability, Non-CRP-Discard Arbiter PUF Based on Delay Difference Quantization," IEEE Transactions on Circuits and Systems—I: Regular Papers, vol. 72, no. 2, pp. 573-585, Feb. 2025.