Circuit Simulation Project

Name of the participant: Bharani J

Title of the circuit: Design and Simulation of Hamming Code (7,4) Error Detection and Correction Circuit Using Logic Gates

Theory/Description:

Hamming Code is a method used for error detection and correction in digital communication and data storage. It adds redundant parity bits to the original data to detect and correct single bit errors. The Hamming (7,4) code takes 4 data bits and adds 3 parity bits, forming a 7-bit code word.

- Data bits: D1, D2, D3, D4
- Parity bits: P1, P2, P3

Parity Bit Generation (Even Parity):

The parity bits are generated using XOR operations as follows:

- P1 is generated using bits 3, 5, and 7
- P2 is generated using bits 3, 6, and 7
- P3 is generated using bits 5, 6, and 7

Error Detection and Correction:

At the receiver side, parity bits are recalculated and compared with the received parity bits to generate syndrome bits:

- S1 checks positions 1, 3, 5, 7
- S2 checks positions 2, 3, 6, 7
- S3 checks positions 4, 5, 6, 7

The syndrome value (S3 S2 S1) represents the binary index of the erroneous bit position. If the syndrome is non-zero, the corresponding bit is inverted to correct the error automatically.

Circuit Diagram(s):

The circuit diagram will be designed using XOR gates and a 3-to-8-line decoder. The error bit will be inverted using XOR gates at the output end. Hence it produces the corrected code.

Results (Input, Output waveforms and/or Multimeter readings):

The proposed Hamming (7,4) code circuit is expected to detect and correct single-bit errors accurately. The results will be verified through simulation.

Source/Reference(s) :

M. Morris Mano, "Digital Design," 6th Edition, Pearson, 2017.
R.W. Hamming, "Error Detecting and Error Correcting Codes," Bell System Technical Journal, vol. 29, pp. 147–160, 1950.