Circuit Simulation Project

https://esim.fossee.in/circuit-simulation-project

Name of the participant : Pandiri Bhanu Sri Venkata Vamsi

Title of the circuit : Design and Implementation of 8-bit LFSR, Bit Swapping LFSR and Weighted Random Test Pattern Generator: A Performance Improvement.

Theory/Description : The power dissipation during the testing cycle is more than that of the normal working of the chip. One reason is that as the chip size is being diminished the power dissemination of the circuit is likewise lessened. Adding a little overhead to the circuit for the purpose of testing which can remove the use of complex external testing component is the method called as Built In Self Test (BIST). In BIST the LFSR is utilized to produce the irregular patterns for testing of a VLSI circuit. This paper describes of a conventional linear feedback shift register, BS-LFSR and multiple WRTPG.

Circuit Diagram(s) :

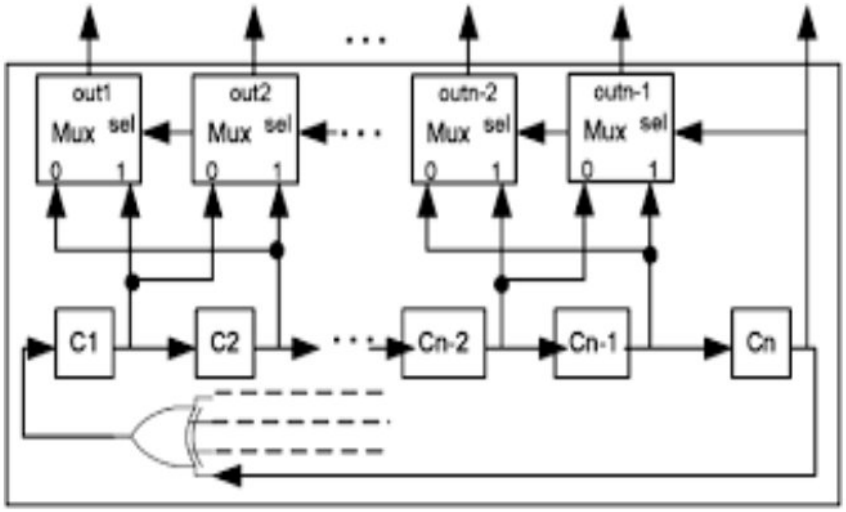
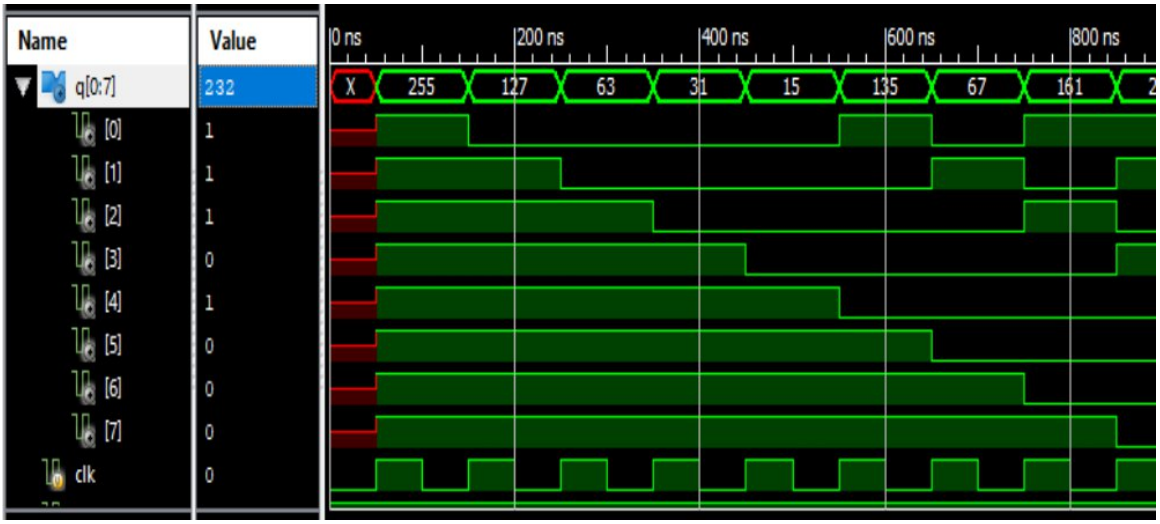


FIGURE 2
ARCHITECTURE FOR BIT SWAPPING LFSR

Results (Input, Output waveforms and/or Multimeter readings) :



Note:- q[0:7] is the output of Random Test Pattern Generator

Source/Reference(s) : https://ieeexplore.ieee.org/document/8908063

[1] A. Bagalkoti, S. B. Shirol, R. S, P. Kumar and R. B. S, "Design and Implementation of 8-bit LFSR, Bit-Swapping LFSR and Weighted Random Test Pattern Generator: A Performance Improvement," 2019 International Conference on Intelligent Sustainable Systems (ICISS), Palladam, India, 2019, pp. 82-86, doi: 10.1109/ISS1.2019.8908063. keywords: {Built-in self-test;Test pattern generators;Power dissipation;Conferences;Circuit faults;Generators;LFSR-Linear Feedback Shift Register;BIST-Built-In Self Test;BSLFSR-Bit-Swapping LFSR;AWRTPG-Arithmetic Weighted Random Test Pattern Generator;CUT-Circuit Under Test},