

Presenter: NARMATHA B

Course: BE(Electronics and Communication Engineering)

Institute: Government College of Technology

Project title – RECONFIGURABLE 10T SRAM WITH COMPUTE IN MEMORY

Reference Research Paper:

Reconfigurable 10T SRAM for Energy-Efficient CAM Operation and In-Memory Computing

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 33, NO. 4, APRIL 2025

Link :

<https://ieeexplore.ieee.org/document/10854884>

Introduction

The 6T SRAM cell uses shared read/write bitlines, offering high speed and compact area but suffering from read disturbance and limited noise margins, making it unsuitable for Compute-in-Memory applications. In contrast, 10T SRAM employs separate read and write paths, eliminating read disturbance and improving stability, making it better suited for CIM despite a slight area overhead.

Existing problem in the reference paper

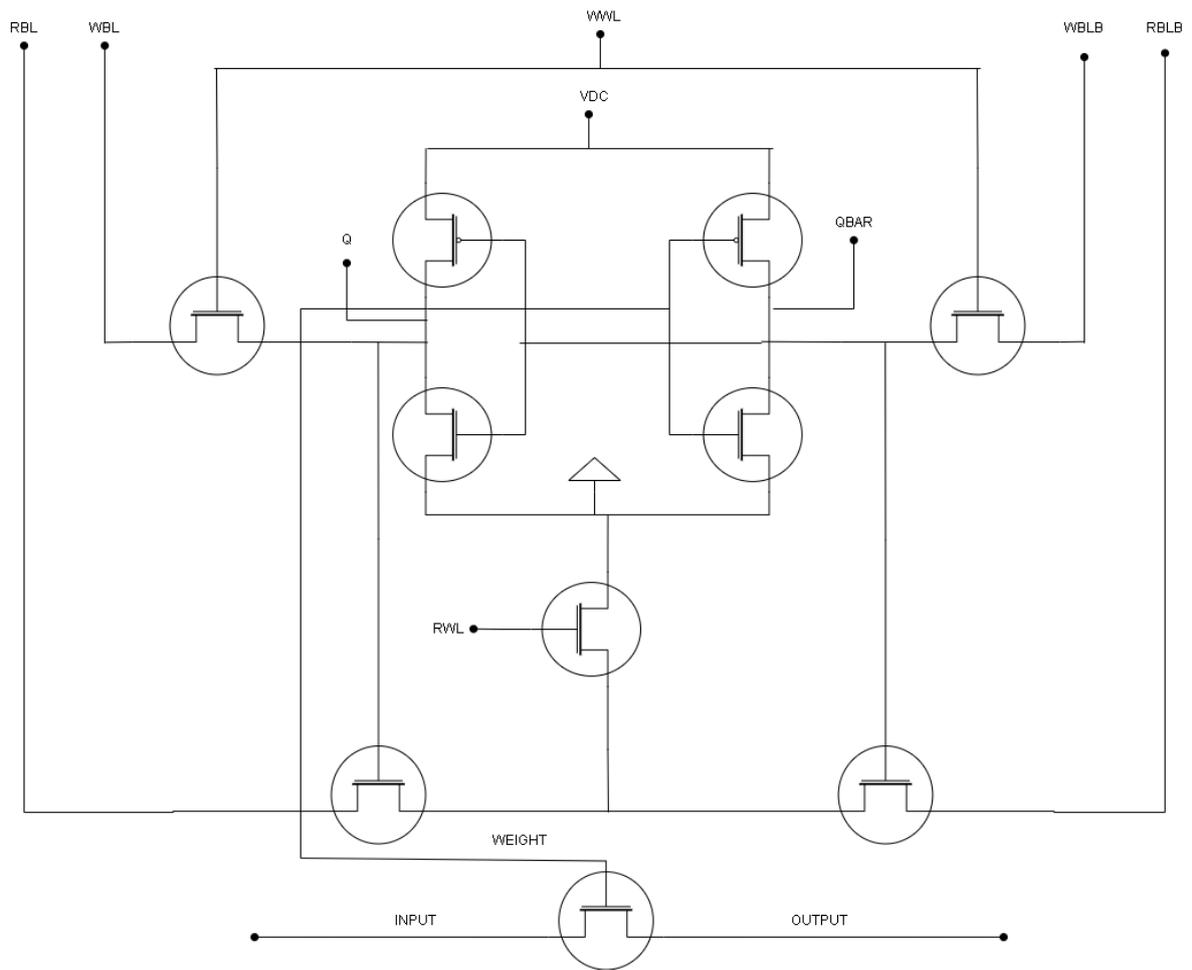
In the existing 10T sram cim cell has diode connected read access transistors causes continuous current flow during read operation, leading to higher static power consumption.

This increases the overall energy consumption of the memory, making it less efficient for low-power consumption.

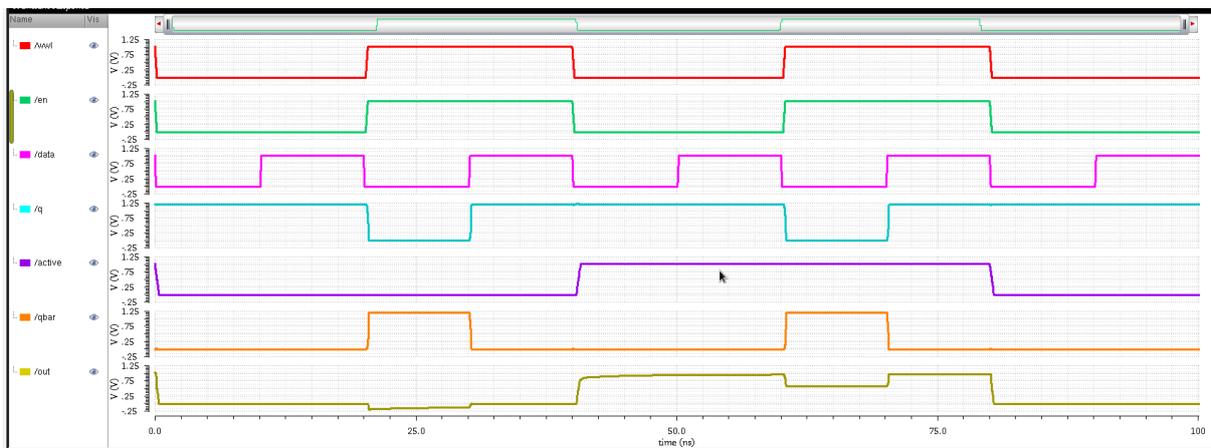
Proposed 10T SRAM CIM CELL

The diode-connected transistor is replaced by an NMOS device with increased threshold voltage to reduce leakage power.

CIRCUIT DIAGRAM:



RESULTS:



WWL-write word line
Data-Sram input

q-sram output(weight)
active-input

output -AND output(CIM)

