Research Migration Project

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Title of the circuit : DELAY ANALYSIS OF APPROXIMATE PARALLEL PREFIX ADDERS

Theory: Approximate Parallel Prefix Adders (APPAs) are high-speed arithmetic circuits designed to reduce computation delay and improve energy efficiency by relaxing exact arithmetic requirements in non-critical bit positions. In conventional exact adders such as Ripple Carry Adders (RCAs) and exact Parallel Prefix Adders (PPAs), carry propagation across all bit positions leads to increased critical path delay, higher wiring complexity, and greater power dissipation, especially for large operand widths.

Recent advances in approximate computing have shown that many applications—including digital signal processing, image and video processing, and machine learning accelerators—can tolerate small arithmetic inaccuracies without noticeable degradation in output quality. APPAs exploit this tolerance by selectively truncating or simplifying carry propagation in the least significant bits (LSBs), thereby significantly reducing the carry chain length.

An APPA architecture is divided into an **approximate region** and an **exact region**. The approximate region reduces delay by suppressing carry propagation, while the exact region employs a **parallel prefix carry computation structure** to preserve correctness in the most significant bits (MSBs). This hybrid approach provides an efficient trade-off between performance and accuracy, making APPAs suitable for modern high-speed digital systems.

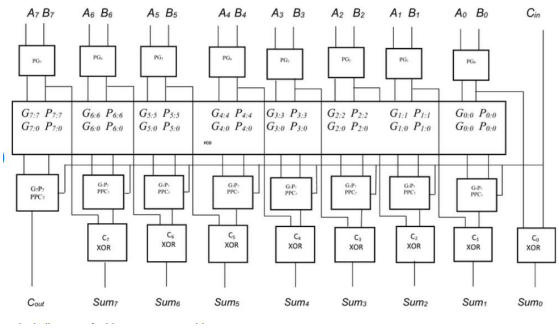
Working Principle: The working principle of an Approximate Parallel Prefix Adder is based on **carry truncation combined with prefix-based carry computation**. Initially, the input operands are converted into **propagate (P)** and **generate (G)** signals, which determine carry behavior at each bit position.

In the approximate region, typically comprising the lower-order bits, carry propagation is intentionally suppressed and the sum is computed using only the propagate signals. This eliminates carry chaining and significantly reduces the critical path delay.e

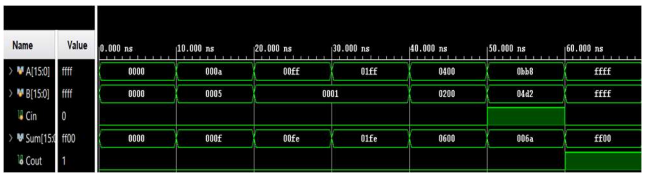
At the boundary between the approximate and exact regions, a **truncated carry signal** is generated and applied to the exact region. The higher-order bits employ a **parallel prefix carry network** with a tree-structured architecture and logarithmic depth to efficiently propagate the carry.

Finally, the sum bits in the exact region are computed by combining the propagate signals with their corresponding carry inputs. By limiting approximation to lower-order bits and preserving exact computation in higher-order bits, the APPA achieves high-speed operation with acceptable numerical accuracy.

Circuit Diagram(s) :



Expected Results (Input, Output waveforms) :



Source/Reference(s) : 1. journal-iiie-india.com/1_sep_23/5_online.pdf

2. https://ijsrd.com/articles/IJSRDV8I10348.pdf

3. https://www.ijraset.com/research-paper/analysis-of-parallel-prefix-adders